Voltage Source Multi Switched Capacitor Boost and Buck-Boost High Gain DC-DC Converters

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***Abstract*—This paper presents dc-dc converters based on multi switched capacitor cells for high boost. The essence in a grid connected micro-inverter is dc-dc converter; it is employed to boost the low PV voltage, which varies from 35-45 V_{DC} in order to increase the bus voltage to be 380-400 V_{DC}. Inverter utilizes this high bus voltage to match the grid voltage, which is 240 V_{AC} at 60 *Hz* frequency. For conventional boost converter, this requires high boost ratio that is beyond its practical capability. Furthermore, the high duty ratio needed will result in high components stress that suppresses the overall efficiency of the converter. To overcome aforementioned problems, this paper suggests the integration of multiple switched-capacitor cells (SCs) with conventional boost and buck-boost converters to achieve high dc-link voltage. Results based on 100 *W* laboratory prototype are given to verify the theoretical analysis.**

***Index Terms*-- High voltage gain, lower duty ratio, multiple switched capacitor (SC) cells, wide input voltage variation**

I. INTRODUCTION

Over the past few decades, photovoltaic (PV) and fuel cell technologies have been gaining popularity among researchers as alternatives to fossil fuel based power generation systems [1-4]. The high step-up Dc–Dc converter is the essence in a photovoltaic (PV) grid connected micro inverter system; it is employed to boost the low PV voltage which is 35-45 V_{DC} to a higher bus voltage around 380-400 V_{DC}. The inverter utilizes this high bus voltage to match the grid voltage which is 240 V_{AC} at 60 *Hz* frequency [1-7]. A simple solution to this is to connect numerous PV or fuel cell units in series, until the required bus voltage level is obtained. This issue has been addressed by authors in [6, 7].

Isolated Dc–Dc converters can be utilized to step up to the required voltage, using high voltage transformer (HVT). In such case, there are two basic techniques to obtain a high voltage gain. First is by increasing the turns ratio of the HVT; and second is to use voltage multiplier circuits on the secondary side of HVT [8-11]. Zero-voltage (ZVS) and (ZCS) Zero-current switching can be easily achieved using the leakage inductance of the HVT in full-bridge converters based on phase-shift pulse width modulation (PWM) control technique [12]. However, HVT with high turns ratio is unattractive for the reason that it magnifies voltage and current spikes in the transformer secondary side, the voltage stress across the output diode becomes much higher than the output voltage, and demands the use of diodes with high breakdown voltage [13]. Moreover, leakage inductance of the transformer induces high circulating current in the primary side, which can possibly, decrease the functional life of PV modules [12], hence large electrolytic capacitors are required to prevent input current ripple, which will increase size and cost of the converter. Consequently, all the disadvantages mentioned associated with isolated converters decrease its overall efficiency [12, 14, 15].

On the other hand, non-isolated dc-dc converter, such as the basic boost converter, suffers from the drawback of high voltage stress on the switch and diode, which are equal to the output voltage, discouraging its implementation in high voltage applications. Moreover, this problem leads to a condition of employing active components with high voltage and diode with fast reverse recovery, effectively, contributing to higher cost. Furthermore, even though the output voltage can theoretically approach infinity, this cannot be achieved experimentally due to the parasitic resistive elements in the converter. Subsequently, some researchers proposed the use of switched capacitor (SC) circuits with basic boost converter to further boost the voltage gain [16]. Nevertheless, the impacts of parasitic elements, which can still affect the practical attainable voltage gain and efficiency of the SC-based boost converter, remain to be investigated.

II. PROPOSED EXTENDABLE SWITCHED (SC) CELL TECHNIQUE DERIVED HIGH GAIN BOOST AND BUCK-BOOST DC-DC CONVERTERS

Proposed *SC*-cell for boost and buck-boost Dc-Dc converters are shown in Fig. 1 (a) and (b). The *N*-stage *SC*-cells for both boost and buck-boost dc-dc converters can be formed by equal number of capacitors and diodes. The *SCs* are connected between the source and the load in such a way that during the *ON* time of the Switch, *SCs* are connected in series to supply the load, while during the *OFF* time of the switch *SCs* are connected in parallel to be charged through the inductor. Furthermore, higher voltage gain is achieved by adding N number of *SC*-cells, so that even at a smaller *ON* time of the switch higher output voltage is achieved compared to the basic boost and buck-boost converters. As a result of reducing the *ON* time of the switch is to achieve lower ripple is produced on the input current, also current ripples of the power devices can be reduced. Due to extreme duty ratio severe rectifier reverse-recovery problem is inherited to the converters. These problems can reduce the overall efficiency of the converter. As the name suggests in Fig. 1 (a) and (b), the boost SC-cell is integrated with the basic boost converter and buck-boost SC-cell is integrated with the basic buck-boost converter, so that the forward boost diodes $D_{Fb1,2,3...N}$ and forward buck-boost diodes $D_{Fbb1,2,3...N}$ are connected in the same direction as the output rectifier diode D_O.

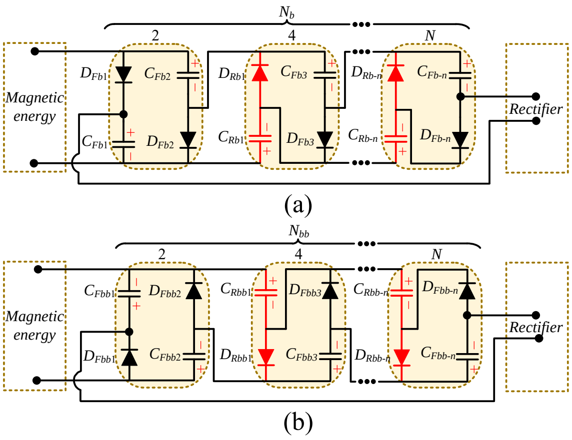


Fig. 1. Proposed extendable *SC*-cells; (a) Boost *SC*-cell, (b) Buck-boost *SC*-cell.

SC-stages can be extended to n number, such that the number of boost *SC*-stages can be extended at the rate of; $N_b = (n_{DRb} - n_{DRb}) + n_{DFb}$ and the number of buck-boost SC-stages can be extended at the rate of; $N_{bb} = (n_{DRbb} - n_{DRbb}) + n_{DFbb}$ where; n_{DFb} and n_{DFbb} represent the total number of forward biased boost and buck-boost diodes. Furthermore, n_{DRb} represents the total number of reverse biased boost diodes and n_{DRbb} represents the total number of reverse biased buck-boost diodes. Therefore, N_b is the total number of boost *SC*-stages and N_{bb} is the total number of buck-boost *SC*-stages.

According to the volt–second balance on the inductor, we have

$$V_G.D.T_S = (VC_{Fb} - V_G)(1-D)T_S = (VC_{Rb} - V_G)(1-D)T_S \quad (1)$$

$$V_G.D.T_S = VC_{Fbb}(1-D)T_S = VC_{Rbb}(1-D)T_S \quad (2)$$

Each forward boost C_{Fb} capacitor connected in the SC network adds up a voltage equal to (3). While, each forward buck-boost C_{Fbb} capacitor connected in the SC network adds up a voltage equal to (4)

$$VC_{Fb} = VC_{Rb} = \left(\frac{V_G}{1-D}\right) \quad (3)$$

$$VC_{Fb} = VC_{Rb} = \left(\frac{V_G D}{1-D}\right) \quad (4)$$

III. Steady State Operation of the Proposed *N*-Stage SC-cell Derived Boost and Buck-Boost DC-DC Converters

The 2-stage *SC*-cell boost and buck-boost converters have also been discussed by authors in [17]. In contrast, to form *n*-stage *SC*-cell, forward capacitors $C_{Fb3}...C_{Fb-n}$, cannot be connected directly with capacitors C_{Fb1} and C_{Fb2}. As seen from Fig. 2, reverse diode $D_{Rb1}...D_{Rb-n}$ and reverse capacitor $C_{Rb1}...C_{Rb-n}$ a (reverse extension) is connected between each (forward extension) of *SC*-cell network.

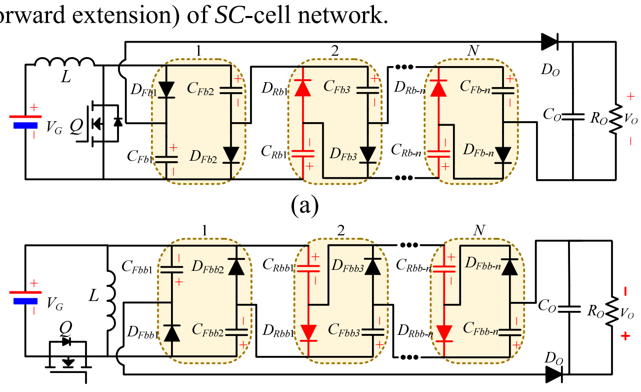


Fig. 2. *n*-Stage *SC* integrated switch mode Dc-Dc converters; (a) boost, (b) buck-boost.

Operating modes for boost and buck-boost *N*-stage *SC*-cells:

When the inductor current is continuous, there are three operating modes for the proposed converters. Fig. 3 shows the key waveforms for *n*-stage *SC*-cell boost and buck-boost dc-dc converters. Where V_{GS} is the driving signal of the switch Q; V_{CFb1}, and V_{CFb2} are the voltages of capacitors C_{Fb1} and C_{Fb2}, respectively; while V_{CRb1} and C_{Fb3} are the voltages of capacitors C_{Rb1} and C_{Fb3} respectively; and i_L is the current of the inductor.

[t_0–t_1]; Mode$_1$: During time [t_0-t], switch Q is conducting, and the input voltage source charges L, and C_{Fb2} charges C_{Rb1}. Meanwhile, C_{Fb3}, C_{Fb2} and C_{Fb1} are in series with the voltage source to supply the load through Q. Thus, voltages of V_{CRb1}, V_{CRb2} and V_{CRb3} decrease.

[t_1–t_2]; Mode$_2$: During time, [t_1-t_2], V_{CRb3} increases while V_{CRb1} decreases. As the voltages of V_{CRb1} and C_{Fb3} become equal before the switch conducts, we have $V_{CRb1} = C_{Fb3}$.

[t_2–T_S]; Mode$_3$: During time, [t_2-T_S], the switch is turned *OFF*. Due to the fact $V_{CRb1} > C_{Fb3}$, D_{Fb3} continues to conduct and D_{Fb2} remains *OFF*. L charges C_{Fb1} via D_{Fb3}, and charges C_{Fb2} and C_{Fb3} via D_{Fb3} while C_{Rb1} discharges. The paths of current flow for *N*-Stage *SC*-cell derived boost Dc-Dc converter are shown in Fig. 4.

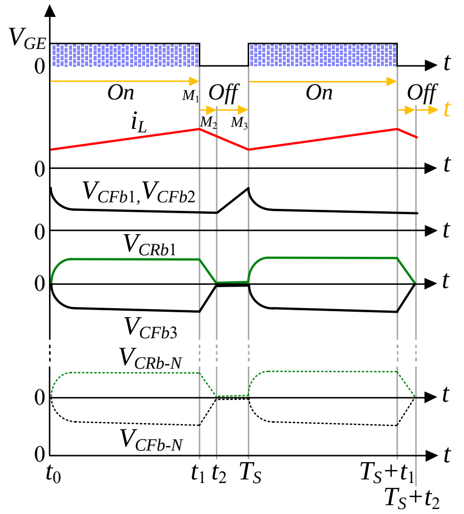
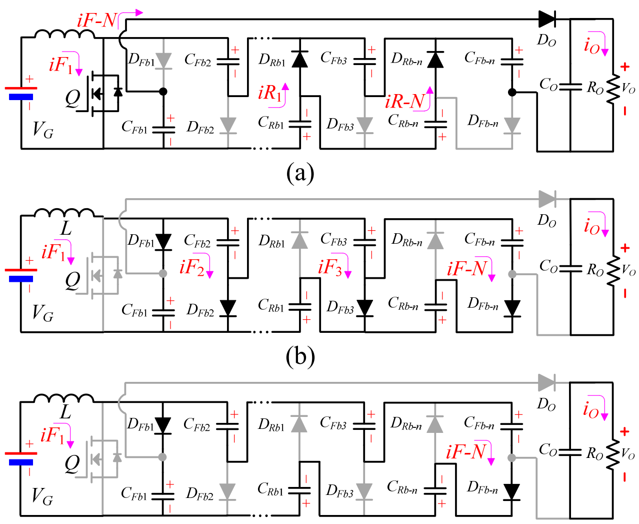


Fig. 3. Steady state operation wave form for *n*-stage *SC*-cell derived boost and buck-boost dc-dc converters.



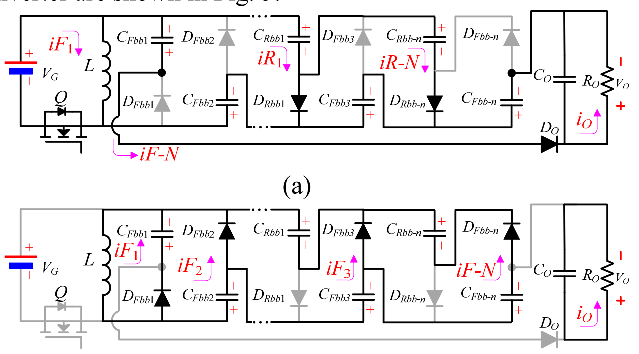
(a)

(b)

(c)

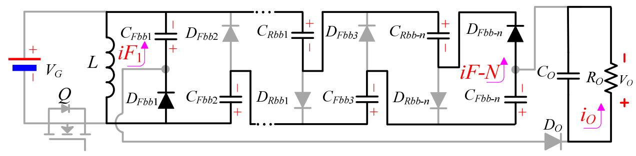
Fig. 4. Current flow for *n* Stage *SC*-cell derived boost Dc-Dc converter, when switch; (a) ON, (b) OFF, (c) OFF.

The description of operating modes for *N*-stage *SC*-cell buck-boost derived Dc-Dc converter is same as *N*-stage *SC*-cell boost derived Dc-Dc converter. Therefore, paths of current flow for *N*-stage *SC*-cell derived buck-boost Dc-Dc converter are shown in Fig. 5.



(a)

(b)



(c)

Fig. 5. Current flow for *n* Stage *SC*-cell derived buck-boost Dc-Dc converter, when switch; (a) ON, (b) OFF, (c) OFF.

Moreover, boost and buck-boost *SC*-cell derived dc-dc converters output voltage; V_{bO} and V_{bbO} is given in (5) and (6) respectively

$$V_{bO} = V_{CFb1} + V_{CFb2} \cdots + V_{CFb(N)} \quad (5)$$

$$V_{bbO} = V_{CFbb1} + V_{CFbb2} \cdots + V_{CFbb(N)} \quad (6)$$

Since no SC-stages are connected to the basic boost and buck-boost converters shown in Fig.2 (a) and (b) respectively, the voltage gain of the boost and the buck-boost converter can be given as (7) and (8) respectively

$$M = \frac{V_O}{V_G} = \left(\frac{1}{1-D}\right) \quad (7)$$

$$M = \frac{V_O}{V_G} = \left(\frac{D}{1-D}\right) \quad (8)$$

Moreover, the voltage gain of the boost SC-cell integrated with the basic boost converter and the voltage gain of the buck-boost SC cell integrated with the basic buck-boost converter can be given as (11) and (12) respectively

$$M = \frac{V_O}{V_G} = \left(\frac{1}{1-D} + \frac{1}{1-D} + \frac{N_b}{1-D}\right) = \frac{2.N_b}{1-D} \quad (11)$$

$$M = \frac{V_O}{V_G} = \left(\frac{D}{1-D} + \frac{D}{1-D} + \frac{N_{bb}}{1-D}\right) = \frac{2D.N_{bb}}{1-D} \quad (12)$$

IV. Testing Parameters for Simulation and Experiment Verification

In order to verify the proposed dc-dc converters, boost converter with 4 *SC*-stages is compared with the basic boost converter in the laboratory by taking the experimental results for both the converters.

TABLE I
TESTING PARAMETERS FOR EXPERIMENT PROTOTYPE

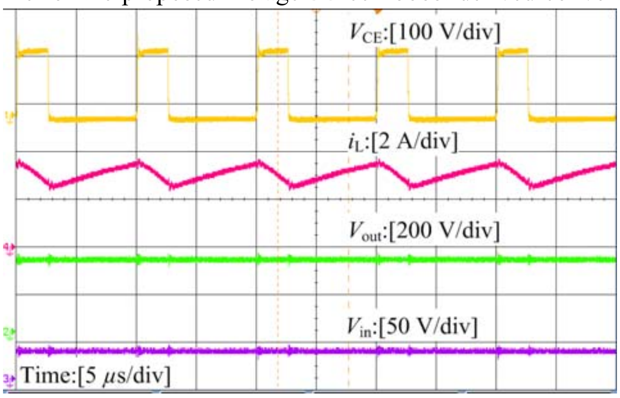
Parameter	4-Stage *SC*-cell derived boost dc-dc converter
V_{IN} *(DC)*	35 and 45
V_{OUT} *(DC)*	380
f s (kHz)	100
WOUT	100

V. Experiment Results

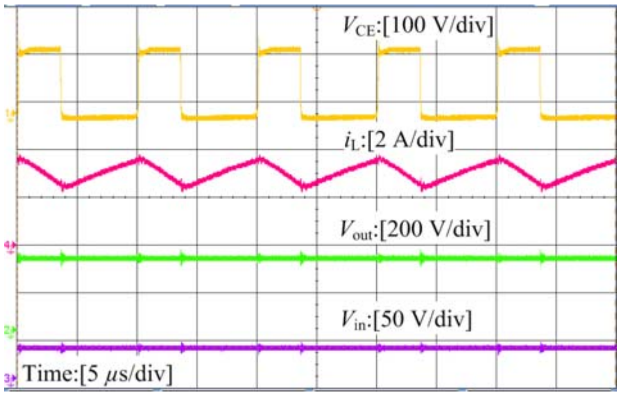
Boost converter extension of *SCs* to *n*-stages shown in Fig 2(a) has a simple circuit configuration and a high voltage gain. Therefore, proposed 4-stage *SC*-cell derived boost dc-dc converter is taken as the example for experiment results. To evaluate the impact of the proposed extendable *SC*-cell techniques. Prototype was fabricated in the laboratory with a full load of 100 *W*. Testing parameters are listed in Table I. Experiment waveforms shown in Fig. 6 (a) and (b) show the voltage stress on switch V_{CE}, input inductor current i_L, output voltage V_O, and input voltage V_{IN}. Fixed output voltage *Vo* of 380 V_{DC} is extracted from input voltage, varied from 35 and 45 V_{DC} at full load 100 *W*, simply by controlling the *ON* time (Duty %) of the switch *Q* as shown in Fig 6 (a)and(b) respectively. When the input voltage was 35 V_{DC}, the *ON* time of the proposed 4-stage *SC*-cell boost derived converter was 73 %. Moreover, when the input voltage was 45 V_{DC} the *ON* time the *ON* time of the proposed 4-stage *SC*-cell boost derived converter was 65 %. It is obvious in Fig 6; the *ON* time for the proposed 4-stage *SC*-cell boost derived converter is less than 75 %. Comparatively, the inductor current ripple Δi_L and turn-*OFF* current of the switch is lower.

As a result of reducing the *ON* time of the switch is to achieve lower ripple is produced on the input current, also current ripples of the power devices can be reduced.

The efficiency of the proposed converter with different input voltages (35 and 45 V_{DC}) is shown in Fig. 7. The output voltage of the proposed converter is regulated at 380 V. The results represent that the proposed converter has lower efficiency at lower input because of higher conducting loss accompanied by higher input current, due to higher ON time of the switch. The highest system efficiency for 45 V_{Dc} input voltage appeared 94.86 % at *Po* = 100 W load.



(a)



(b)

Fig. 6. Experiment results of proposed boost converter with 4 *SC*-stages; (a) 35 Vin to 380 Vout, (b) 45 Vin to 380 Vout.

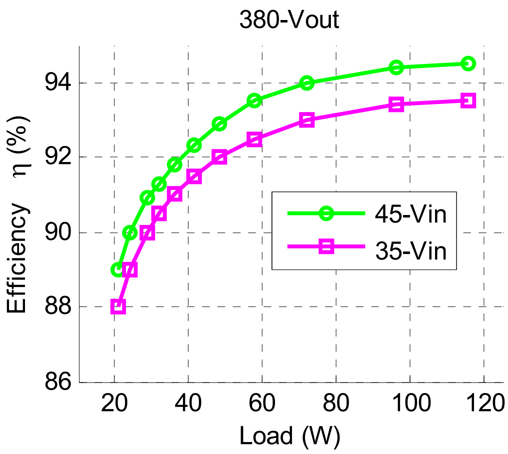


Fig. 7. Efficiency comparison between proposed boost converter with 4 *SC*-stages in Fig. 6(a).

VI. Conclusion

This paper, proves that the voltage gain of the boost converter with proposed 4-stage *SC*-cell is higher than the basic boost converter for the same duty ratio, at the cost of lower efficiency as the *SC*-cell stages are increased, which is due to increase in component count. However if the objective is to obtain the same voltage gain, the 4-stage *SC*-cell boost based converter gives the same gain at a lower duty ratio, resulting in increase of efficiency compared with the basic boost converter. Even though the cost of 4-stage SC based boost converter is higher than that of a basic boost converter, it allows the extension of the voltage gain that would otherwise not be practically viable with the basic boost. Furthermore, the difference in terms of efficiency for basic boost compared with 4-stage *SC* based boost converter is quite marginal, especially for practical duty in the range of 0.5-0.8. All this assures the suitability of *SC*-based boost-converter to replace basic boost converter for high voltage gain application.

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