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Data Compression Device based on Modified LZ4 Algorithm

Weiqiang Liu, Senior Member, IEEE, Faqiang Mei, Chenghua Wang, Maire O'Neill, Senior Member, IEEE and Earl E. Swartzlander, Jr., Life Fellow, IEEE

Abstract-Data compression is commonly used in NAND flashbased Solid State Drives (SSDs) to increase their storage performance and lifetime as it can reduce the amount of data written to and read from NAND flash memory. Software based data compression reduces SSD performance significantly and, as such, hardware-based data compression designs are required. This paper studies the latest lossless data compression algorithm, *i.e.*, the LZ4 algorithm which is one of the fastest compression algorithms reported to date. A data compression FPGA prototype based on the LZ4 lossless compression algorithm is studied. The original LZ4 compression algorithm is modified for real-time hardware implementation. Two hardware architectures of the modified LZ4 algorithm (MLZ4) are proposed with both compressors and decompressors, which are implemented on a FPGA evaluation kit. The implementation results show that the proposed compressor architecture can achieve a high throughput of up to 1.92Gbps with a compression ratio of up to 2.05, which is higher than all previous LZ algorithm designs implemented on FPGAs. The compression device can be used in high-end SSDs to further increase their storage performance and lifetime.

Index Terms—Solid-State Drives (SSDs); Lossless compression; LZ algorithms; LZ4; FPGA

I. INTRODUCTION

C OLID-state drives (SSDs) based on NAND flash memory A have become popular in consumer electronic devices such as smart phones, tablet and desktop systems [1-2]. It is highly desirable to reduce the amount of data in SSDs and the read/write data transmission time to/from SSDs as flash memory has a finite number of program-erase (P/E) cycles thus limited lifetime [3]. For example, older single-level cell (SLC) NAND-flash memory was able to withstand 150,000 P/E cycles, while multi-level cell (MLC) NAND-flash memory using 15-19nm process technologies wears out after only 3,000 P/E cycles [2], [4]. Furthermore, the performance of MLC flash memory is also much slower than that of its SLC counterpart. Also, more advanced triple-level cell NAND flash memory has an even lower number of P/E cycles [5]. This problem is expected to worsen with further scaling of the semiconductor process. Therefore, to increase the lifetime and also the

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W. Liu, F. Mei and C. Wang are with the College of Electronic and Information Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing, Jiangsu, China (e-mail: {liuweiqiang, meifaqiang, chwang}@ nuaa.edu.cn).

M. O'Neill is with Center for Secure Information Technologies, Queen's University Belfast, Belfast, UK (e-mail: m.oneill@ecit.qub.ac.uk).

E. E. Swartzlander, Jr. is with the Department of Electrical and Computer Engineering, University of Texas at Austin, USA (e-mail: eswartzla@aol.com). performance of flash-based SSDs, the amount of data written to and read from the SSDs should be reduced, which can be achieved using data compression. Another benefit of using lossless data compression in SSDs is to reduce the I/O latency.

Data compression for SSDs has been widely adopted. Data compression can be implemented in three layers: the application, the file system or the firmware of the storage device. Most data compression algorithms are adopted in the application layer and the file system using software implementation. Software based data compression can be useful in improving the lifetime of SSDs. However, the overall performance of SSDs is reduced significantly due to the slow compression and decompression speed. A recent study [6] based on realistic data and systems show that applying data compression in the firmware of the SSDs using a data compression hardware accelerator is the best approach. A typical SSD architecture with data compression acceleration is shown in Fig. 1.

Although hardware-based compression is required for NAND flash memory and SSDs, little research has been conducted on how to design a high performance hardware compression accelerator [7-13]. In [6], it was found that for high-end SSDs with transaction rates of up to 3K per second, compression/decompression rates of above 200MB/s (*i.e.*, 1.6Gbps) are required. However, existing designs are limited in performance with compression speeds in the range of 0.567Gbps~1.6Gbps [7-13], which cannot meet the requirement of high-end SSDs.

In this paper, the design of a hardware accelerator based on the latest lossless data compression algorithm, *i.e.*, LZ4 [14] for data compression in high-end SSDs is studied and demonstrated on an FPGA device. The original LZ4 algorithm is somewhat difficult to implement in hardware as it was proposed for software implementation. It is not possible to store all the text in calculating the hash. Its output delay is uncertain and the input data is limited by the address width of the hash table. As a result, the LZ4 algorithm has been modified for hardware



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implementation in this paper to solve these problems. By using the MLZ4 algorithm, the hash computation is improved for the compression ratio and low output latency is achieved. The implementation results on an FPGA platform show the proposed MLZ4 architecture provides the highest throughput performance compared with previous FPGA implementations of LZ algorithms, which makes it suitable for high-end SSDs.

The paper is organized as follows: Section II reviews lossless data compression algorithms and their hardware implementations. The original LZ4 algorithm is also reviewed in this section. Section III presents the modified LZ4 algorithm. Two hardware architectures of both the MLZ4 compressors and decompressors are proposed in Section IV. A comparison with other FPGA hardware designs of LZ algorithms is provided in Section V. Section VI concludes the paper.

II. REVIEW

A. Data Compression Algorithms and Implementations

There are two main categories of data compression, namely, lossy and lossless compression [15]. As lossy compression allows loss of accuracy to an acceptable level, it is usually used for multimedia applications where errors can be tolerated [16]. Lossless compression can compress and then recover the data from compressed data without loss of information; and it is used for applications where even one single bit difference between the original and reconstructed data cannot be tolerated.

The applications of lossless data compression have been increasing significantly due to both the demand for increased bandwidth [17-18] and the need to improve storage capacity [3]. Lossless data compression has been successfully deployed in storage systems including tapes, hard disk drives, SSDs, file servers and storage area networks (SAN).

Lossless data compression can be achieved using two different approaches: statistical model based compression such as Huffman coding [19] and dictionary based compression including the Lempel-Ziv (LZ) algorithms [20-21]. The LZ algorithms belong to adaptive dictionary based techniques, which are the most popular lossless compression algorithms when prior statistical characteristics of the data are unknown. The LZ algorithms have been adopted by many compression format standards such as Zip, GNU zip and Zlib [22].

LZ algorithms were proposed by Jacob Ziv and Abrahm Lempel in 1977 [20] and 1978 [21] in their two landmark papers. These papers presented two different approaches. The approach based on the 1977 paper is referred to as the LZ77 (or LZ1) family which includes LZ77, LZRW [23], LZSS [24], LZMA [11] *et. al.* LZ77 algorithms use a sliding window to examine the input sequence. Its principle is to find whether the sequence being compressed appears in the previously input data. If so, a pointer is used to point to the repeated strings. The dictionary refers to a portion of the previously encoded sequence. The approaches based on the 1978 paper are known as the LZ78 (or LZ2) family which includes LZ78, LZW [25], *et. al.* LZ78 algorithms create a dictionary of phrases from the input data. When a match with the phrases that have appeared in the

dictionary occurs, the encoder will output the phrase's index in the dictionary rather than the phrase itself.

Yann Collet proposed the LZ4 algorithm in 2011 [13-14], which is a variant of LZ77. The compression speed of a LZ4 software implementation is shown to be fastest among the LZ algorithms. However, there is little research conducted on the hardware implementation of LZ4 as it is much younger than other LZ algorithms. Hardware designs of lossless data compression algorithms are receiving increase attention due to the exponential expansion in network communication and data storage. FPGA implementations of LZ algorithms such as LZRW3 [12], LZW [8], [10], the Lempel-Ziv-Markov chain algorithm (LZMA) [11] and LZ4 [13] have been proposed to meet real-time requirements. Thus, it is necessary to study hardware architectures of LZ4 in order to explore its performance for consumer electronic applications such as SSDs.

B. A Review of the LZ4 Algorithm

This subsection reviews the LZ4 algorithm. Its data format and data flow are introduced. The shortcomings of the original LZ4 algorithm and data format are also discussed.

LZ4 was initially defined as a form of compressed data format. Compressed data files are composed of LZ4 sequences that include a token, literal length, offset, and match length as shown in Fig. 2. The token is used to indicate the length of unmatched and matched characters. The literal length indicates the length of uncompressed data and its value is equal to the value of the length of uncompressed data minus 15. The uncompressed data is stored as literals in the LZ4 sequence and it is copied from the original data. When the input data finds data that appeared before via searching, this data will be compressed. The value of the offset indicates the address of the current data minus the address of the prior data. Match length means the length of the matching data.

The operation of the LZ4 algorithm is mainly divided into the following five steps [14]: hash computation, matching, backward matching, parameter calculation and data output, which is shown in Fig. 3.

III. THE MODIFIED LZ4 ALGORITHM

An improved data format is proposed in this section along with an improved algorithm to solve the defects in the original LZ4 algorithm.

The original LZ4 algorithm was proposed for software implementation in general processors. As such, there are some issues with the LZ4 algorithm for hardware implementation:

- The hash calculation is only performed for unmatched characters. Hash calculation is not applied to the backward matching. Thus, part of the matching data's hash value will not be calculated.
- 2) For Step 2 of the original LZ4 algorithm, when there is hash conflict (different data have the same hash value),

Token	Literal Length	Literals	Offset	Match Length
1 Byte	0-n Bytes	0-L Bytes	2 Bytes	0-n Bytes

Fig. 2. Data format of an LZ4 sequence.



Fig. 3. The flow chart of original LZ4 algorithm.

more clock cycles are needed to recalculate the hash value, which reduces the compression speed.

- 3) The input data is limited by the address width in the hash table. The maximum number of memory addresses in the hash table is the maximum size of the input data. It cannot compress data constantly.
- 4) Output delay is uncertain. According to the original LZ4 data format, the length of matched characters and unmatched characters should be obtained before outputting the data. For example, if the unmatched character length is 40k bytes, data can only be outputted after all 40k bytes are searched.

In order to increase the compression speed in hardware, the LZ4 data format is changed as shown in Fig. 4. Note that the format of the token and offset is consistent with the original format. The main differences are as follows:

Literal Length: If the value of the first four bits of the token is less than 15, there is no literal length. If the value of the first four bits of token is 15, the length of unmatched literals is the sum of all literal lengths.

Match length: If the value of the last four bits of the token is less than 15, there is no match length. The value of the actual match length is the value of the last four bits of token plus 4. If the value of the last four bits of the token is 15, the value of the match length is represented using 2 bytes after the offset. The actual value of the match length is the sum of them.

The modified LZ4 (MLZ4) algorithm (addressing the issues mentioned above) is detailed as follows:

- 1) To improve the compression ratio, the hash value of the data can be calculated during the backward matching in the modified algorithm to exploit the parallelism of hardware implementation.
- 2) To reduce the delay when a hash conflict occurs and to improve the compression speed, a hash dictionary that corresponds to the hash table is added. The difference between the hash table and the hash dictionary is that the hash table stores the address, while the hash dictionary

stores the corresponding data based on the hash value. During match searching, the data stored in the hash dictionary can be read and compared when reading the address at the same time. As a result, the number of clock cycles can be reduced.

- 3) To allow continuous compression in hardware, a Valid Bit is added in the hash table. When the data is valid, the Valid Bit is set to '1'. When the data is invalid in a hash table, the Valid Bit is reset to '0' and a data cleaning process is also added. In this way, when the data address reaches the maximum address and continues to search for backward matching, no matching error occurs, as there will be no overlapped address. Thus, continuous compression can be achieved.
- 4) To make sure the output delay is predictable, the LZ4 data format is changed as shown in Fig. 4. When the unmatched character length is longer than 300 bytes, the backward match is ignored. For the above mentioned example, if the length of the unmatched characters is 40k bytes, the data can be output when the match length reaches 300 bytes according to the new data format. Thus, the waiting time for matching is reduced significantly.

A flow chart illustrating the operation of the MLZ4 algorithm is shown in Fig. 5.

Token	Literals	Literal Length	Literals	Literal Length	 Offset	Match Length
1 Byte	0-15 Bytes	0-1 Byte	0-128 Bytes	0-1 Byte	 2 Bytes	0-2 Bytes

Fig. 4. The data format of MLZ4.



Fig. 5. The flow chart of MLZ4 algorithm.



IV. FPGA ARCHITECTURE AND IMPLEMENTATION OF THE MLZ4 ALGORITHM

Compared with software, a hardware implementation offers parallel processing that can allow multiple compressors to work at the same time to increase the throughput of compression. The FPGA implementation of the MLZ4 algorithm is presented in this section with two FPGA hardware architectures, *i.e.*, MLZ4-1 and MLZ4-2, with both compressors (*i.e.*, MLZ4C-1 and MLZ4C-2) and decompressors (*i.e.*, MLZ4D-1 and MLZ4D-2).

A. The 1st FPGA Architecture of MLZ4 Compressor (MLZ4C-1)

The 1st hardware architecture of the LZ4-1 compressor is shown in Fig. 6. It mainly consists of the input RAM, the output RAM, word shift register, reading back control module (*i.e.*, Ref. Control), search module (including Hash Engine, Word Table, Hash Table, Hash Clear, Match and Backward Match), literal length calculation module (*i.e.*, Literal Length), match length calculation module (*i.e.*, Match Length) and output control module (including Ports A, B and C Control).

The input and output RAM modules store the data before and

after compression both in a 64k RAM. Data are read from the input RAM and then turned into 32-bit data through the word shift register. The 32-bit data is fed to the Hash Engine to compute the hash value. The Ref. Control module controls the reading pointer to read the data, and then uses them to find the backward matching data.

The search module performs the hash value calculation, reads the Hash Table. It also changes the Ref. address, finds any matching conflicts, judges the match length, calculates the offset and judges whether the input data address (denoted as IP) has reached the end.

Literal and match length calculation modules are used to calculate the length of the unmatchable characters and matching data. The Port A and B Control modules write the compressed data to the output RAM according to the MLZ4 data format. The Port C Control module is used to control the compressed data from the Output RAM to the PCI-E interface.

The designs in this work are all implemented on a FPGA evaluation kit. The MLZ4C-1 runs at a frequency of 100MHz and its throughput is 0.8Gbps. The hardware resources used in implementing the compressor are summarized in Table I.



Fig. 8. The hardware architecture of the MLZ4C-2 compressor.



Fig. 9. The hardware architecture of the MLZ4D-2 decompressor.

Compression results from testing the proposed designs with benchmark files from the Calgary corpus (paper1 and paper2) [26], the Canterbury corpus (asyoulik and cp) [26] and the Silesia corpus (dickens) [27] are shown in Table II. It can be seen that the compression ratio achieved is between 1.65 and 2.05.

B. The 1st FPGA Architecture of the MLZ4 Decompressor (MLZ4D-1)

The decompressor is simpler than the compressor. The information contained in token and literal length show the length of unmatched characters. The unmatched character can be output directly and the positions of offset and match length can be calculated according to the length of unmatched characters. Matched strings can be copied from decompressed data based on the values of offset and match length. All data can be decompressed after repeating the above operations. The decompressor of the MLZ4D-1 is also designed and

implemented on a FPGA chip. Its hardware architecture is shown in Fig. 7. The decompressor mainly includes three modules: the input control module, the IP control module and the output control module. The Input RAM is used to store the data. The IP control module changes IP according to literal length, offset and match length. The output control module is used to control the storage of decompressed data and output the final data.

The MLZ4D-1 decompressor can run much faster than the MLZ4C-1 compressor as LZ4 is an asymmetric compression algorithm. In this work, the MLZ4D-1 operates at 120MHz and its throughput is 0.96Gbps. The hardware resources used by the MLZ4D-1 design are also summarized in Table I.

C. The 2nd FPGA Architecture of the MLZ4 Compressor (MLZ4C-2)

The 2nd hardware architecture of the LZ4 compressor is shown in Fig. 8. The main difference between MLZ4C-1 and

MLZ4C-2 are the search module and the output module. Additionally, MLZ4C-2 includes a new IP Shift block. The detailed differences are as follows:

The search module: The Match block in MLZ4C-2 is divided into Word Compare, Match Compare and IP Compare blocks. Furthermore, the Backward Match block is divided into Backward Compare and Match Flag blocks. Therefore, the critical path of both the match and backward match logic is further reduced by inserting pipeline registers.

The output module: The even and odd output bits are written into RAM-A and RAM-B, respectively, by using two RAM blocks. Both RAM blocks can output the data at the same time. The even bits are in the 8 most significant bits of the output data, *i.e.*, dzip[15:8], and the odd bits are in the 8 least significant bits, *i.e.*, dzip[7:0], which is in the revised format as shown in Fig. 4.

The MLZ4C-2 design runs at a frequency of 240MHz and its throughput is 1.92Gbps. The hardware resources used in implementing the compressor are summarized in Table III. Test results show that the compression ratios achieved by the MLZ4C-2 design are the same as that listed in Table II.

D. The 2nd FPGA Architecture of the MLZ4 Decompressor (MLZ4D-2)

The MLZ4D-2 is similar to MLZ4D-1, as shown in Fig. 9. However, the input module that includes IP calculation, Input Control and Input RAM blocks is now replaced with a FIFO. The IP Control block in MLZ4D-1 is changed to a Read Control block in MLZ4D-2, where the combinational logic has been further divided and pipeline registers have been added to increase the performance.

The MLZ4D-2 operates at 260MHz and its throughput is up to 2080Mbps. The hardware resources used by the decompressor are also summarized in Table III.

TABLE I
RESOURCES USED FOR BOTH 1 ST COMPRESSOR (MLZ4C-1) AND 1 ST
DECOMPRESSOR (MI $74D-1$)

Resource	MLZ4C-1	MLZ4D-1	Total
Slices	571	365	936
FFs	605	604	1,209
LUTs	1,302	767	2,069
BRAMs	76.5	32.5	109

TABLE II						
Test Original Compressed Compression						
Files	Size (Bytes)	Size (Bytes)	Ratio			
paper1	53,161	28,686	1.85			
paper2	82,199	46,750	1.76			
asyoulik	125,179	75,467	1.66			
ср	24,603	11,993	2.05			
dickens	10,192,446	6,161,433	1.65			

TABLE III
RESOURCES USED FOR 2 ND COMPRESSOR (MLZ4C-2) AND 2 ND DECOMPRESSOR
(MLZ4D-2)

Resource	MLZ4C-2	MLZ4D-2	Total	
Slices	345	155	500	
FFs	937	377	1314	
LUTs	573	342	915	
BRAMs	69	20	89	
DSPs	4	0	4	

E. Comparison between MLZ4-1 and MLZ4-2

Due to the optimized pipelined architecture, the 2nd design is much faster than the 1st design. The throughput of MLZ4C-2 and MLZ4D-2 are 2.4 and 2.16 times that of MLZ4C-1 and MLZ4D-1, respectively. At the same time, the hardware required is also reduced significantly. MLZ4C-2 only uses 60% of the slices and 90% of the BRAMs used in MLZ4C-1. However, MLZ4C-2 uses 4 additional DSPs. MLZ4D-2 uses much fewer slices compared with MLZ4D-1, where more than half of slices are saved. The number of BRAMs used is also reduced by over 38%. The comparison results show that the second architecture is a much better design. Both MLZ4-1 and MLZ4-2 are further compared with previous work in the following section.

V. COMPARISON WITH OTHER FPGA IMPLEMENTATIONS OF LZ ALGORITHMS

In this section the proposed designs are compared with other LZ algorithm FPGA implementations. The designs compared include X-MatchPROv4 [7] using the XMatchPRO algorithm, the conventional LZW [8], the ELDC-3 core [9] that implements four image compression algorithms, an improved LZW VLSI Processor [10] which implements the New LZW algorithm, LZMA [11], the LZWR3 Core [12] that implements the LZRW3 algorithm and a LZ4 FPGA device [13].

The comparison is summarized in Table IV. The MLZ4C-1 is a baseline design. Its performance is not so attractive compared with the previous best design. However, the revised and pipelined design, *i.e.*, MLZ4C-2, has improved the compression performance significantly. From the table, it is clear that the proposed MLZ4C-2 offers the highest performance. Although it consumes slightly more slices, MLZ4C-2 increases the compression throughput by 20% compared with the best previous design in [13] which is also an LZ4 FPGA design, as shown in Fig. 10. The main difference between MLZ4C-2 and the design in [13] is that a Word Table added in MLZ4C-2 is used to find both the matched address and the matched data at the same time, which reduces the delay; the output module uses two RAM blocks; all combinational modules are further divided and registers are inserted to pipeline the design.

MLZ4C-2 also outperforms (over 47% faster) the leading commercial compression device, *i.e.*, LZRW3 [12]. MLZ4D-2 is also the fastest decompressor compared with other state-of-the-art designs. This confirms that the proposed MLZ4-2 design is the fastest compression device, and hence, is suitable for high-end SSDs.

VI. CONCLUSION

This paper presents a modified LZ4 algorithm and its FPGA implementations. Several aspects of the original LZ4 algorithm are modified for efficient hardware implementation. These changes improve both the compression and decompression speeds. The implementation on a FPGA chip shows that the proposed designs can achieve compression and decompression throughputs of up to 1.92Gbps and 2.08Gbps, which is 20% and

TABLE IV

Compression Device	Algorithms	FPGA Technology	Complexity	Clock Speed (MHz)	Troughput (Gbps)
X-MatchProv4 [7]	X-MatchPRO	180nm	5367 LUTs	50	0.567 (Compression)
LZW [8] ELDC-3 Core [9]	LZW CGF, GZIP, ELIC, PNG	120nm/150nm 90nm	332 Slices 631 LUTs 247 Slices 474 LUTs 5900 Slices	50 75	0.700 (Compression) 1.120~1.282 (Decompression) 0.400~0.528 (Compression)
Improved LZW Processor [10]	New LZW	90nm	3218 Slices 272 Kb RAMs	124	1.587 (Compression)
LZMA [11]	LZMA	40nm	NA	125	0.604 (Compression)
LZRW3 Core [12]	LZRW3	28nm	227 Slices 789 FFs 4~36 BRAMs	210	1.300 (Compression)
LZ4 [13]	LZ4	28nm	266 Slices 17 BRAMs 3 DSPs	200	1.600 (Compression)
MLZ4C-1			571 Slices	100 (Compression)	0.800
MLZ4D-1	Modified LZ4	28nm	365 Slices 32 5 BRAMs	(Decompression)	(Decompression)
MLZ4C-2	Modified L74	28nm	345 Slices 69 BRAMs 4 DSPs	240 (Compression)	1.920 (Compression)
MLZ4D-2			155 Slices 20 BRAMs	260 (Decompression)	2.080 (Decompression)

47% faster than the previous best compressor and decompressor designs respsectively. The proposed MLZ4 and its hardware architectures can therefore be used to increase the storage performance and lifetime of high-end SSDs.



Fig. 10. Performance Comparison with state-of-the-art LZ compressors.

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Weiqiang Liu (M'12-SM'15) received the B.Sc. degree in Information Engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China and the Ph.D. degree in Electronic Engineering from the Queen's University Belfast (QUB), Belfast, UK, in 2006 and 2012, respectively. In Dec. 2013, he joined the College of Electronic and Information

Engineering, NUAA, where he is currently an Associate Professor. He was a Research Fellow in the Institute of Electronics, Communications and Information Technology (ECIT) at QUB from Aug. 2012 to Nov. 2013. He has published one research book by Artech House and over 50 leading journal and conference papers. His paper was finalist in the Best Paper Contest of IEEE ISCAS 2011 and he is the coauthor of a Best Paper Candidate of ACM GLSVLSI 2015. He serves as an Associate Editor of IEEE Transactions on Computers (TC), the leader of The Multimedia Team at TC Editorial Board, and the Guest Editors of two special issues of IEEE Transactions on Emerging Topics in Computing. He has been a technical program committee member for several international conferences including ARITH, ASAP, ISCAS, and ICONIP. He is a member of IEEE CASCOM Technical Committee. His research interests include VLSI design for digital signal processing and cryptography, and emerging technologies in computing systems.



Faqiang Mei received the B.Sc. degree in Information Engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2016. He is currently a Master student in Circuit and Systems, College of Electronic and Information Engineering, NUAA. His research interest includes FPGA design for

lossless data compression algorithms, and cryptographic hardware.



Chenghua Wang received the B.Sc. and M.Sc. degrees from Southeast University, Nanjing, China, in 1984 and 1987, respectively. In 1987, he joined the College of Electronic and Information Engineering, Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, where he became a full Professor in 2001. He has published 6 books and over 100 technical papers in journals and conference proceedings. He is the recipient of more than ten teaching and research awards at the provincial and ministerial level. His current research interests include testing of integrated circuits, and circuits & systems for communications.



Maire O'Neill (M'03-SM'11) obtained an M.Eng. degree with distinction and a Ph.D. in Electrical and Electronic Engineering from Queen's University Belfast (QUB) in 1999 and 2002 respectively. She is currently Research Director of the Centre for Secure Information Technologies (CSIT) at QUB. She previously held a prestigious

UK Engineering and Physical Sciences Research Council (EPSRC) Leadership Fellowship (2008-2015) and was a former holder of a UK Royal Academy of Engineering (RAEng) research fellowship (2003-2008). She has received numerous awards for her research to date which include a 2014 UK Royal Academy of Engineering Silver Medal, the Women's Engineering Society (WES) prize at the 2006 IET Young Woman Engineer of the Year awards and she was named British Female Inventor of the Year in 2007. She has authored two research books and has over 125 international peer-reviewed conference and journal publications. She is Associate Editor for IEEE Transactions on Computers and IEEE Transactions on Emerging Topics in Computing and has acted as guest editor for a number of journals, including the IET Information Security (2005) launch issue and a special issue on 'Cryptography in the coming decade' in ACM Trans. on Embedded Computing (2015). She has been a technical program committee member for many international conferences, including DAC, CHES, DATE, SOCC, ISCAS, IET ISSC and RFIDSec. She is an IEEE Circuits & Systems for Communications (CASCOM) Technical committee member and was treasurer of the Executive Committee of the IEEE United Kingdom and Ireland (UKRI) Section, 2008-09. She is a member of the Royal Irish Academy and a Fellow of the Irish Academy of Engineering.



Earl E. Swartzlander Jr. (SM'79-F'88-LF'11) received the B.S. degree from Purdue University in 1967, the M.S. degree from the University of Colorado in 1969, and the Ph.D. degree from the University of Southern California in 1972, all in electrical engineering. He is a professor of electrical and computer engineering at the University of Texas at Austin. In this position, he and his

students conduct research in computer engineering with emphasis on application-specific processor design, including high-speed computer arithmetic, embedded processor architecture, VLSI technology, and nanotechnology. As of December 2016, he has supervised 46 Ph.D. students. He is the author of two books, editor of 11 books and the author or coauthor of 86 refereed journal papers, 41 book chapters, and 310 conference papers. He was the editor-in-chief of the *IEEE Transactions on Computers* from 1990 to 1994 and was the founding editor-in-chief of the *Journal of VLSI Signal Processing*. In addition, he has served as an associate editor for the *IEEE Transactions on Computers*, the *IEEE Transactions on Parallel and Distributed Systems*, and the *IEEE Journal of Solid-State Circuits*. He has been a member of the Board of Governors of the IEEE Computer Society (1987-1991), the IEEE Signal Processing Society (1992-1994), and the IEEE Solid-State Circuits Council/Society (1986-1991). He has been a member of the IEEE History Committee (1996-2004), the IEEE Fellows Committee (2000-2003), the IEEE James H. Mulligan, Jr., Education Medal Committee (2007-2011), the IEEE Awards Planning and Policy Committee (2011-2013), the

IEEE Awards Board Awards Review Committee (2014-2016), the IEEE Awards Board (2015-2016), and the IEEE Awards Policy and Portfolio Review Committee (2017). He has chaired a number of conferences. He is a life fellow of the IEEE and has been honored with the IEEE Third Millennium Medal, the Distinguished Engineering Alumnus Award from the University of Colorado, the Outstanding Electrical Engineer and Distinguished Engineering Alumnus Awards from Purdue University, and the IEEE Computer Society Golden Core Award.