Generalized Class-E Power Amplifier with Shunt Capacitance and Shunt Filter

Generalized Class-E Power Amplifier With Shunt Capacitance and Shunt Filter

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***Abstract*— This paper presents a generalized analysis of the Class-E power amplifier (PA) with a shunt capacitance and a shunt filter, leading to a revelation of a unique design flexibility that can be exploited either to extend the maximum operating frequency of the PA or to allow the use of larger active devices with higher power handling capability. The proposed PA fulfills zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions, resulting in a theoretical dc-to-RF efficiency of 100%. Explicit design equations for the load-network parameters are derived, and the analytical results are confirmed by harmonic-balance simulations. Two PA prototypes were constructed with one designed at low frequency and the other at high frequency. The first PA, which employs a MOSFET and a lumped-element load-network, delivered a peak drain efficiency (*DE*) of 93.3% and a peak output power of 37 dBm at 1 MHz. The second PA, which employs a GaN HEMT and a transmission-line (TL) load-network to provide the drain of the transistor with the required load impedances at the fundamental frequency as well as even and odd harmonic frequencies, delivered a peak *DE* of 90.2% and a peak output power of 39.8 dBm at 1.37 GHz.**

***Index Terms*— Class E, GaN, harmonic suppression, harmonic tuning, high efficiency, lumped element, MOSFET, power amplifier (PA), series reactance, shunt capacitance, shunt filter, transmission line.**

I. Introduction

THE CLASS-E power amplifier (PA) with shunt capacitance and series filter, introduced by Ewing [1] and further analyzed by Sokal and Sokal [2] and Raab [3], has been widely used due to its simple topology and high-efficiency operation. The high efficiency is achieved by applying zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions, producing a soft switching at the OFF-to-ON transition. One of the main drawbacks of this topology is that it employs an ideal RF choke (RFC), which in practice needs to be replaced by a large, hence lossy and bulky, inductor. An improved variant of this PA topology with a finite dc-feed inductance instead of an RFC is reported in [4]–[8], also known as "Class E with parallel circuit."

Subsequently, the Class-E PA with series inductance and shunt filter, with switch voltage and current waveforms being the duals to those in the Class-E PA with shunt capacitance and series filter, hence termed as "inverse Class E," is introduced in [9] and [10]. In contrast to its predecessor, it adopts zero current switching (ZCS) and zero current derivative switching (ZCDS) conditions, producing a soft switching at the ON-to-OFF transition. Although it offers 20% lower peak switch voltage than that in [1]–[3] as well as has the ability to absorb device output inductance (L_{out}), its implementation is limited to small-to-medium power levels as it does not inherently incorporate a shunt capacitance to absorb device output capacitance (C_{out}). For simplicity, the "Class-E PA with shunt capacitance and series filter" and the "Class-E PA with series inductance and shunt filter" will be referred to as "Class E" and "inverse Class E," respectively, hereinafter.

Another high-efficiency PA topology, i.e., the Class-E PA with shunt capacitance and shunt filter depicted in Fig. 1(a) is introduced in [11]. A similar variant shown in Fig. 1(b) disposing the need for the capacitance C_X placed in parallel with the shunt filter and load resistance is described in [12]. These two topologies adopt ZVS and ZVDS conditions, and importantly, incorporate both shunt capacitance C to absorb C_{out} as in the Class E and series inductance L to absorb L_{out} as in the inverse Class E, rendering it attractive for high-frequency implementations where device parasitics play a dominant role in deleteriously affecting the PA performance. Furthermore, in series-filter-based Class-E topologies such as [1]–[8], a large inductance value is required to implement the series filter, whereas in shunt-filter-based Class-E topologies such as [9]–[13], the value of the inductor that forms the shunt filter is considerably lower for the same loaded quality factor value. A large inductance is typically accompanied with a large parasitic equivalent series resistance (ESR) and a low self-resonant frequency (SRF), hence rendering the series-filter-based Class-E topologies unattractive.

In this paper, we present a generalized Class-E PA with shunt capacitance and shunt filter, which incorporates a series reactance X as illustrated in Fig. 1(c). The system of equations describing the behavior of this PA is derived and expressed in terms of parameter q, whose value can be chosen arbitrarily, leading to an infinite number of solutions for the load-network

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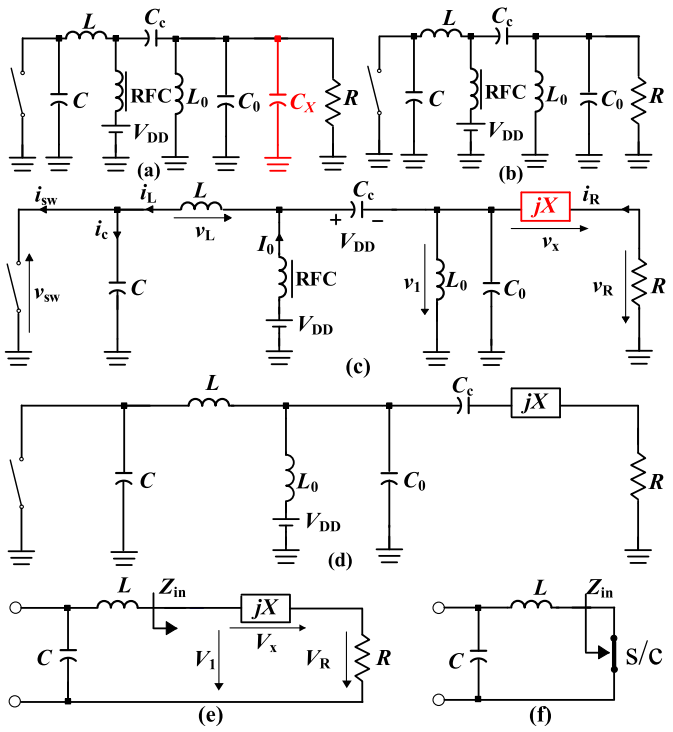

Fig. 1. Class-E PA with shunt capacitance and shunt filter. (a) Circuit topology in [11]. (b) Circuit topology in [12]. (c) Generalized circuit topology proposed in this paper. (d) As in (c) but without RFC. (e) Equivalent load-network of (c) and (d) at the fundamental frequency. (f) Equivalent load-network of (c) and (d) at harmonic frequencies.

parameters. For example, $q = 1.6$ results in $X = 0\ \Omega$ reducing the circuit in Fig. 1(c) to that in Fig. 1(b) [12], whereas $q = 1.3$ results in $X = -32.67\ \Omega$ reducing the circuit in Fig. 1(c) to that in Fig. 1(a) [11] with the series connected jX and R transformed into the parallel connected C_X and R. Therefore, the solutions given in [11] and [12] are in fact subsets of the solutions presented in this paper, hence termed as "generalized Class-E PA with shunt capacitance and shunt filter." Furthermore, the maximum operating frequencies (f_{max}) of the foregoing PAs are strictly constrained by C_{out}. The f_{max} of the PAs in [6], [7], [11], and [12] are, respectively, 1.57, 1.65, 1.44, and 1.91 times higher than that of the classical Class-E PA in [1]–[3]. It will be shown through theoretical analysis and practical design examples that the generalized Class-E PA with shunt capacitance and shunt filter proposed in this paper can be operated to provide even higher f_{max} than that of [12] that is already higher than that of [6], [7], and [11].

In summary, the advantages of the proposed PA over those in [1]–[8] are as follows.

1) It has the ability to absorb the transistor output inductance, which, if not taken into account in the analysis, will have a detrimental impact on the PA performance at high frequencies.
2) The inductance value of the shunt filter L_0 is much lower than that of the series filter for the same loaded quality factor, leading to a reduced loss due to a smaller ESR.
3) The inductor L_0 of the shunt filter can double as a dc-feed inductance, meaning that the circuit in Fig. 1(c) can be simplified to that in Fig. 1(d) by removing the RFC, resulting in a more compact circuit.
4) It can be operated at higher frequencies (for a given transistor), or alternatively, at higher output power levels (for a specified operating frequency).
5) As will be shown later in this paper, its peak switch voltage does not vary as much as that in [7] as q increases (to permit higher frequency or higher power operations).

Furthermore, the chief contributions of this paper are as follows:

1) expanding the design space of the Class-E PA with shunt capacitance and shunt filter introduced in [11], [12] by providing a continuum of operating modes through parameter q, hence offering more degrees of freedom in the design;
2) providing insights into design tradeoffs between different circuit parameters;
3) presenting a transmission-line (TL) load-network that not only fulfills the operational conditions of the proposed PA but also facilitates excellent harmonic suppression, thereby reducing the total harmonic distortion of the PA.

The remainder of this paper is organized as follows. Section II describes the circuit analysis in details including the derivation of the system of equations whose solutions provide a comprehensive understanding of how circuit parameters relate to each other. Section III highlights the technical merits of the proposed PA through comparison with the classical Class-E PA. Section IV covers the implementation of two circuit prototypes: the first circuit employs a MOSFET with a lumped-element load network operating in the MF-band, whereas the second circuit employs a GaN HEMT with a TL load network operating in the L-band. Section V lists all research findings derived from this paper.

II. Circuit Analysis

The load-network of the generalized Class-E PA with shunt capacitance and shunt filter, depicted in Fig. 1(c), consists of a shunt capacitance (C), a series inductor (L), a shunt parallel resonator (L_0C_0), a series reactance (X), an RFC, a dc blocking capacitor (C_c), and a load resistance (R). In practice, C can represent the transistor output capacitance and external circuit capacitance added by the load network, L can be used to absorb the transistor output inductance and parasitic lead inductance, and X can be inductive, capacitive as in [11], or zero as in [12]. The drain of the transistor is biased through the RFC, which has infinite reactance at the fundamental frequency (f_0) as well as harmonic frequencies. However, the inductor L_0 of the shunt filter can also be used as a finite dc-feed inductance as shown in Fig. 1(d), thus eliminating the need for a bulky and lossy RFC which poses a major problem in implementations at high frequencies. In the case where X is capacitive, the dc-blocking capacitor C_c in Fig. 1(d) is no longer required and can be removed, further simplifying the circuit topology. Tuned at f_0, the L_0C_0 circuit provides an open circuit at f_0 and short-circuit terminations

at $n \times f_0$. As a result, the PA load-network at f_0 and $n \times f_0$ reduces to that shown in Fig. 1(e) and (f), respectively.

To simplify the analysis of the generalized Class-E PA with shunt capacitance and shunt filter, we adopt the same assumptions used in [12].

The idealized optimum (nominal) Class-E switching conditions are given as follows:

$$v_{\rm sw}(\omega t)|_{\omega t=2\pi} = 0 \tag{1}$$

$$\left.\frac{dv_{\rm sw}(\omega t)}{d\omega t}\right|_{\omega t=2\pi} = 0 \tag{2}$$

where $v_{\rm sw}(\omega t)$ is the voltage across the switch.

Let the sinusoidal fundamental-frequency voltage $v_1(\omega t)$ across the shunt L_0C_0 filter be expressed as follows:

$$v_1(\omega t) = V_1 \sin(\omega t + \varphi_1) \tag{3}$$

where V_1 is the fundamental-frequency voltage amplitude and φ_1 is the phase shift due to a complex load.

When the switch is turned ON for $0 \le \omega t \le \pi$, the voltage across the switch is

$$v_{\rm sw}(\omega t) = V_{\rm DD} - v_{\rm L}(\omega t) - v_1(\omega t) = 0 \tag{4}$$

where $v_L(\omega t)$ is the voltage across the series inductor. Using (7)–(13) from [12] and substituting V_1, i.e., the voltage across the series connection of the reactance X and load R (instead of the voltage V_R across the load R as in [12] where $X = 0\ \Omega$), a general nonhomogeneous second-order differential equation for the switch voltage $v_{\rm sw}(\omega t)$ is obtained

$$\omega^2 LC\frac{d^2v_{\rm sw}(\omega t)}{d(\omega t)^2} + v_{sw}(\omega t) - V_{\rm DD} + V_1\sin(\omega t + \varphi_1) = 0. \tag{5}$$

The normalized general solution of (5) is given as

$$\frac{v_{\rm sw}(\omega t)}{V_{\rm DD}} = C_1\cos q\omega t + C_2\sin q\omega t + 1 + \frac{q^2}{1-q^2}\frac{V_1}{V_{\rm DD}}\sin(\omega t + \varphi_1) \tag{6a}$$

where q is defined as

$$q = \frac{1}{\omega\sqrt{LC}} \tag{6b}$$

and coefficients C_1 and C_2 are obtained by substituting V_R in (17) and (18) of [12] with V_1. It is worth noting here that parameter q in (6b) has different physical meaning from q in [7], where L is connected in parallel with the transistor (instead of in series as in this paper).

For a prescribed supply voltage $V_{\rm DD}$, (6a) contains three unknown parameters q, $V_1/V_{\rm DD}$, and φ_1. Parameter q is treated as a variable and the other two parameters $V_1/V_{\rm DD}$ and φ_1 are determined from a system of two equations resulting from applying the two optimum conditions, i.e., ZVS and ZVDS, given in (1) and (2). Fig. 2 shows the dependency of parameters $V_1/V_{\rm DD}$ and φ_1 on q, from which it can be seen that for $q = 1.607$, $\varphi_1 = -41.6°$ and $V_1/V_{\rm DD} = 0.925$, which agree with the results presented in (20)–(22) of [12].

The normalized switch voltage and current waveforms calculated for $q = 1.3$ (as in [11]), 1.6 (as in [12]), 1.85 (as in the design example later treated in Section III), and 2.1 are shown in Fig. 3, where the switch voltage waveforms satisfy the optimum Class-E conditions for all q values. As q increases, the peak switch voltage does not vary as much as that in [7] while the current waveform changes its shape dramatically, creating a spike at the end of the turn-ON interval as in [7]. In ideal amplifier design, no power is being dissipated within the switch as nonzero voltage and current do not occur simultaneously (Fig. 3). However, in practice, this is something that design engineers must keep an eye on, especially when a slow switching device is used.

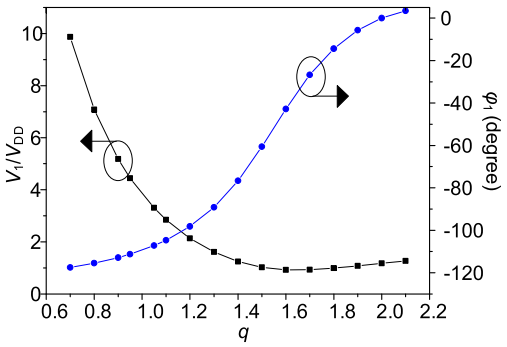

Fig. 2. Optimum Class-E parameters $V_1/V_{\rm DD}$ and φ_1 versus q.

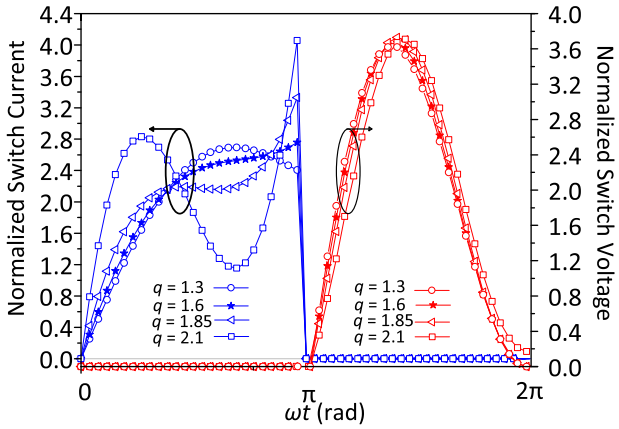

Fig. 3. Normalized switch voltage and current waveforms.

For an idealized amplifier, the dc power $P_0 = I_0V_{\rm DD}$ is equal to the fundamental-frequency output power delivered to the load $P_{\rm out} = V_R^2/2R$, resulting in unity drain efficiency (DE). Hence, the optimum load resistance R can be calculated as

$$R = \frac{1}{2}\frac{V_{\rm R}^2}{P_{\rm out}} = \frac{1}{2}\left(\frac{V_{\rm R}}{V_{\rm DD}}\right)^2\frac{V_{\rm DD}^2}{P_{\rm out}}. \tag{7}$$

The optimum load-network parameter ωL is derived using [12, eqs. (23), (24)] with V_R in (24) replaced by V_1. Subsequently, ωC can be derived from (6b)

$$\omega L = \frac{V_{\rm DD}^2}{2\pi P_{\rm out}}\left[\frac{\pi^2}{2} - \frac{V_1}{V_{\rm DD}}(2\sin\varphi_1 + \pi\cos\varphi_1)\right] \tag{8}$$

$$\omega C = \frac{1}{q^2\omega L}. \tag{9}$$

In the presence of a nonzero reactance X in series with load resistance R, as shown in Fig. 1(e), the real and imaginary

components of voltage amplitude V_1 need to be defined. In this case, the sinusoidal voltage $v_1(\omega t)$ in (3) can be expressed as

$$\begin{aligned} v_1(\omega t) &= v_R(\omega t) + v_X(\omega t) \\ &= V_R \sin(\omega t + \varphi) + V_X \cos(\omega t + \varphi) \end{aligned} \tag{10}$$

where φ is the initial phase.

The ratio of the imaginary and real components of V_1, i.e., V_X and V_R, respectively, can be obtained as follows:

$$q_1 = \frac{V_X}{V_R} = \frac{X}{R} = \tan(\varphi_1 - \varphi) = \tan\psi \tag{11}$$

resulting in

$$V_1 = \sqrt{V_R^2 + V_X^2} = V_R\sqrt{1 + q_1^2} \tag{12}$$

where voltage amplitude V_R is defined in [12, eq. (12)].

As a result, the remaining unknown parameters q_1, V_R/V_{DD}, and φ can be determined as a function of parameter q from a system of three equations of [12, eqs. (2), (3), (19)]. For a prescribed supply voltage V_{DD} and output power P_{out}, the load-network parameters ωL, X, R, and ωC, normalized to V_{DD} and P_{out}, can be expressed in terms of q.

The normalized optimum series inductance $\omega L P_{out}/V_{DD}^2$, series reactance XP_{out}/V_{DD}^2, shunt capacitance $\omega C V_{DD}^2/P_{out}$, and load resistance RP_{out}/V_{DD}^2 are plotted versus parameter q in Fig. 4. From Fig. 4(a), it can be observed that a larger value of ωL corresponds to a lower q value. To compensate for such an increased inductive value, the reactance X must, therefore, be decreased. The series reactance X changes from negative to positive values (or from capacitive to inductive) as q increases. Fig. 4(b) shows that as q increases, the value of ωC increases, and consequently for a specific value of C representing the device output capacitance ($C = C_{out}$), f_{max} increases with the increasing q. Thus, f_{max} of the generalized Class-E PA with shunt capacitance and shunt filter can be expressed as in the following equation:

$$f_{max} = k\frac{P_{out}}{V_{DD}^2 C_{out}}. \tag{13a}$$

The parameter k is plotted versus q in Fig. 4(b), from which it follows that $q = 1.3$ results in $k = 0.0728$ and $q = 1.6$ results in $k = 0.097$, that are in line with [11, Table 3] and [12, eq. (32)], respectively, and are 1.44 and 1.91 times higher than that in [3], respectively. Furthermore, $q = 2.1$ results in $k = 0.227$ with the corresponding f_{max} being 4.5 and 2.7 times higher than that in [3] and [7], respectively. Equation (13a) can be rearranged to calculate the required shunt capacitance C in Fig. 1(d) for a prescribed supply voltage V_{DD}, output power P_{out}, and operating frequency f_0. Thus, the increase in k as q increases can also mean that a larger transistor with higher output capacitance can be used to implement the PA, thus enabling higher output power

$$C = k\frac{P_{out}}{V_{DD}^2 f_0}. \tag{13b}$$

The maximum operating frequency of the PA can also be defined in terms of the transistor output inductance, (13c), using (6b) and (13a). Since k increases with increasing q, m will decrease with increasing q. As a result, for a given

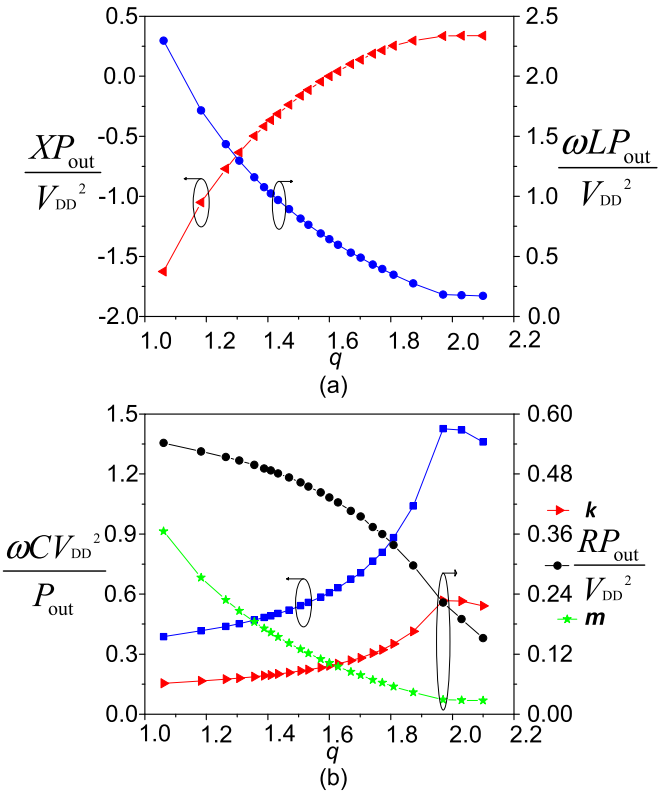

Fig. 4. Normalized optimum load-network parameters for the generalized Class-E with shunt capacitance and shunt filter. (a) Normalized series reactance and inductance. (b) Normalized shunt capacitance and load resistance.

TABLE I
LOAD-NETWORK PARAMETERS OF [11] AND [12] COMPARED TO THIS PAPER

Parameter	Fig. 1(a)		Fig. 1(b)	
	[11]	This work	[12]	This work
q	1.3	1.3	1.6	1.6
k	0.0728	0.07194	0.097	0.097
XP_{out}/V_{DD}^2	− 0.65	− 0.634	0	0
$\omega LP_{out}/V_{DD}^2$	1.32	1.296	0.6351	0.6351
$\omega CV_{DD}^2/P_{out}$	0.455	0.452	0.6096	0.6096
RP_{out}/V_{DD}^2	0.494	0.507	0.4281	0.4281
Switch voltage peak factor	3.63	3.632	3.677	3.677

V_{DD}, P_{out}, and L_{out}, f_{max} will also decrease with increasing q. Parameter m is plotted in Fig. 4(b)

$$f_{max} = \frac{1}{k(2\pi q)^2}\frac{V_{DD}^2}{P_{out}L_{out}} = m\frac{V_{DD}^2}{P_{out}L_{out}}. \tag{13c}$$

Table I shows that for $q = 1.3$ and 1.6, the normalized load-network parameters and switch voltage peak factor derived in this paper are in line with the results obtained in [11] for $q = 1.3$ and in [12] for $q = 1.6$; thus, [11] and [12] are subsets of the work presented in this paper.

III. EXPLORING THE NEW DESIGN SPACE

To accentuate the significance of the theoretical analysis and insights described in Section II, we designed and simulated three distinctive PAs: the Class E with series filter and ideal

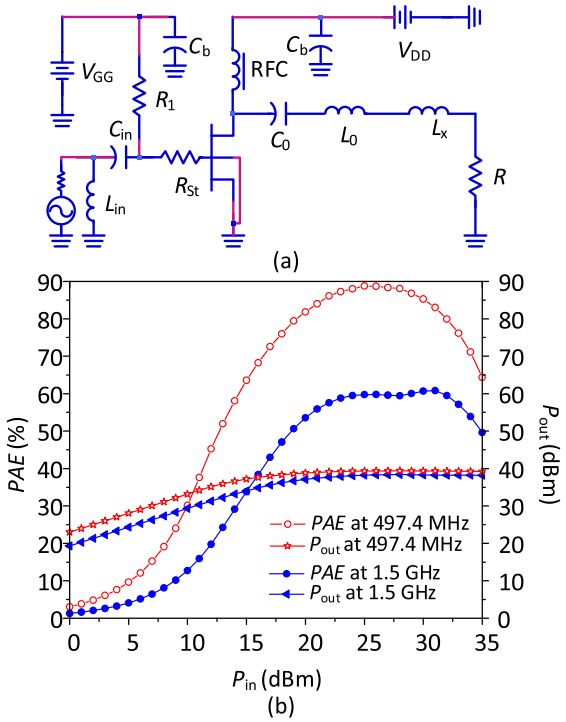

Fig. 5. Class-E PA with series filter and ideal RFC [1]–[3]. (a) Simulated circuit schematic. (b) Simulated PA performance versus P_{in} at 497.4 MHz and 1.5 GHz with $V_{DD} = 28$ V and $V_{GG} = -2.7$ V.

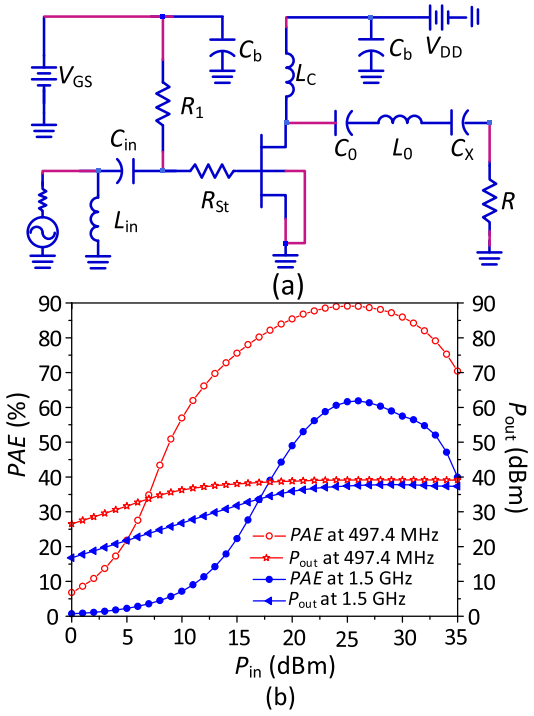

Fig. 6. Class-E PA with series filter and finite RFC [7]. (a) Simulated circuit schematic. (b) Simulated PA performance versus P_{in} at 497.4 MHz and 1.5 GHz with $V_{DD} = 28$ V and $V_{GG} = -2.7$ V.

RFC [1]–[3], the Class E with series filter and finite RFC [7], and the proposed Class E with shunt filter and nonzero X in Fig. 1(c). For fair comparison, the three PAs employ the same transistor, i.e., Cree CGH40010F GaN HEMT with an output capacitance C_{out} of 1.3 pF and an output inductance L_{out} of 0.653 nH, and are biased with the same voltages, i.e., $V_{DD} = 28$ V and $V_{GG} = -2.7$ V. The PAs were designed to deliver an output power of 10 W at a fixed operating frequency $f_0 = 1.5$ GHz.

A. Class-E PA With Series Filter and Ideal RFC [1]–[3]

The design equations in [3] are used to determine the load-network parameters of the PA shown in Fig. 5(a). It follows that $R = 45.2\ \Omega$, $L_X = 5.53$ nH, $C = 0.43$ pF, $L_0 = 48$ nH, and $C_0 = 0.23$ pF for a loaded quality factor $Q_L = 10$. Notice that the required C is smaller than C_{out}. The total series inductance used in the simulation is $L_X + L_0 - L_{out} = 52.9$ nH, i.e., to alleviate the detrimental effect of the parasitic inductance L_{out} on the PA performance. Fig. 5(b) shows that the PA delivers a peak power added efficiency (*PAE*) of 60.9% and a peak P_{out} of 38.4 dBm at 1.5 GHz. Substantially, higher peak *PAE* of 88.9% and peak P_{out} of 39.4 dBm are obtained if the PA is designed at its maximum operating frequency $f_{max} = 497.4$ MHz, calculated using (13a) with $k = 0.0507$ [3], with the circuit component values as follows: $R = 45.2\ \Omega$, $L_X = 16.7$ nH, $C = 1.3$ pF ($= C_{out}$), $L_0 = 145$ nH, and $C_0 = 0.7$ pF for $Q_L = 10$. Thus, to fulfill the optimum Class-E conditions and, consequently, high-efficiency operation, the classical Class-E PA in [1]–[3] should be operated at frequencies below or equal to f_{max} where the relationship $C_{out} \leq C$ holds.

B. Class-E PA With Series Filter and Finite RFC [7].

The design set for maximum operating frequency ($q = 1.468$) in [7, Table VI] is used to determine the load network parameters of the PA in Fig. 6(a). It follows that $R = 104.4\ \Omega$, $L_C = 7.3$ nH, $C = 0.71$ pF, $C_X = 6.39$ pF, $L_0 = 110.8$ nH, and $C_0 = 0.1$ pF for $Q_L = 10$. Notice that the required C is greater than that of the design in Section III-A but smaller than C_{out}. Fig. 6(b) shows that the PA achieves a peak *PAE* of 61.9% and a peak P_{out} of 37.8 dBm at 1.5 GHz.

Substantially higher peak *PAE* of 89% and peak P_{out} of 39.15 dBm are obtained if the PA is designed at f_{max} of [1]–[3], i.e., 497.4 MHz, given that the same q value (i.e., 1.468) results in $C = 2.15$ pF.

C. Proposed Class-E PA With Shunt Filter

Fig. 7(a) shows the simulated circuit schematic of the proposed topology in Fig. 1(c). The value of $q = 1.85$ is selected to give $C = 1.272$ pF $\approx C_{out}$ at $f = 1.5$ GHz, extracted from Fig. 4(b), which results in $k = 0.1496$, extending the f_{max} of the Class E with series filter [1]–[3] by a factor of 2.9. The value of $L = 2.66$ nH is obtained from Fig. 4(a) for $q = 1.85$ and $f = 1.5$ GHz, resulting in an excess inductor $L_e = L - L_{out} \approx 2$ nH. For the given V_{DD} and P_{out}, $X = 20.4\ \Omega$ and $R = 25.1\ \Omega$ are determined from Fig. 4(a) and (b), respectively. Fig. 7(b) shows that the PA achieves a peak *PAE* of 84.3% and a peak P_{out} of 39 dBm at 1.5 GHz.

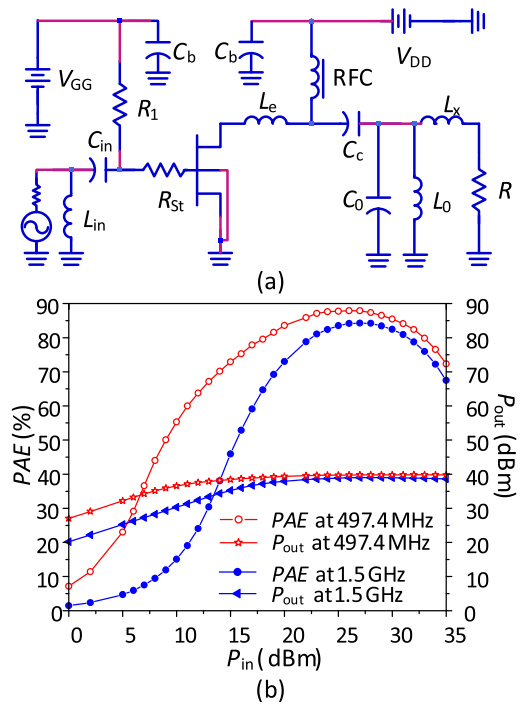

Fig. 7. Proposed Class-E PA with shunt filter. (a) Simulated circuit schematic. (b) Simulated PA performance versus P_{in} at 497.4 MHz and 1.5 GHz with $V_{DD} = 28$ V and $V_{GG} = -2.7$ V.

If designed at f_{max} of [1]–[3], i.e., 497.4 MHz, the same q value (i.e., 1.85) results in $C = 3.84$ pF. Fig. 7(b) shows that the PA achieves a peak PAE of 87.9% and a peak P_{out} of 39.9 dBm. This result also shows that at a fixed frequency, $f = 497.4$ MHz, a larger (hence, higher power capability) transistor with a $C_{out} = 3.84$ pF can be used for this PA design.

The values of L_0 and C_0 in Fig. 7(a) are determined using (14b) and (14c) with the series connected L_X and R transformed to its equivalent parallel circuit L_P and R_P. For a given Q_L, the total inductance L_T that is formed by the parallel combination of L_0 and L_P can be calculated using the following equation:

$$L_T = \frac{R_p}{\omega_0 Q_L} \tag{14a}$$

$$L_0 = \frac{L_P L_T}{L_P - L_T} \tag{14b}$$

$$C_0 = \frac{1}{\omega_0^2 L_0}. \tag{14c}$$

D. Discussion

The optimum circuit component values and performances of the PAs in Section III-A–III-C are summarized and compared in Table II. It has been shown that unlike the classical Class-E PAs in [1]–[3], and [7], the proposed PA can be operated at much higher frequencies while maintaining the high-efficiency characteristics. Critically, the classical PA requires much higher inductance value (L_0) for the same loaded quality factor, rendering its implementation challenging as high inductance implies high ESR and low SRF, meaning that substantial power will be dissipated within the series filter.

TABLE II
PA COMPARISONS

Design Frequency	Class E with Series Filter and Ideal RFC (IIIA)	Class E with Series Filter and Finite RFC (IIIB)	Class E with Shunt Filter (IIIC)
497.4 MHz	C = 1.3 pF L_X = 16.7 nH R = 45.2 Ω L_0 = 145 nH C_0 = 0.7 pF	C = 2.15 pF L_C = 22.1 nH R = 104.4 Ω C_X = 19.27 pF L_0 = 334.1 nH C_0 = 0.306 pF	C = 3.84 pF L = 8 nH R = 25.1 Ω L_X = 6.52 nH L_e = 7.37 nH L_0 = 1.45 nH C_0 = 70.6 pF
	PAE = 88.9% P_{out} = 39.4 dBm	PAE = 89% P_{out} = 39.1 dBm	PAE = 87.9% P_{out} = 39.9 dBm
1.5 GHz	C = 0.43 pF L_X = 5.53 nH R = 45.2 Ω L_0 = 48 nH C_0 = 0.23 pF	C = 0.71 pF L_C = 7.3 nH R = 104.4 Ω C_X = 6.39 pF L_0 = 110.8 nH C_0 = 0.1 pF	C = 1.3 pF L = 2.66 nH R = 25.1 Ω L_X = 2.16 nH L_e = 2 nH L_0 = 0.48 nH C_0 = 23.4 pF
	PAE = 60.9% P_{out} = 38.4 dBm	PAE = 61.9% P_{out} = 37.8 dBm	PAE = 84.3% P_{out} = 39 dBm

TABLE III
LOAD-NETWORK PARAMETERS OF PA PROTOTYPE 1

q	XP_{out}/V_{DD}^2	$\omega LP_{out}/V_{DD}^2$	$\omega CV_{DD}^2/P_{out}$	RP_{out}/V_{DD}^2
1.364	–0.4617	1.1139	0.4835	0.486
1.831	0.2448	0.3485	0.8559	0.34

The Class-E PA with series filter treated in Section III-A employs an ideal RFC that has infinite impedance at all frequencies, and consequently, the series inductors $L_0 + L_X$ can be used to absorb the transistor output inductance L_{out}.

However, in practice, the RFC needs to be replaced with a finite dc-feed inductance, and consequently, L_{out} can no longer be absorbed by $L_0 + L_X$, as L_{out} is no longer in series with $L_0 + L_X$. Similarly, in the Class-E PA with series filter and finite RFC treated in Section III-B, L_{out} cannot be absorbed by L_0. On the contrary, the Class-E PA with shunt filter proposed in this paper has a mechanism in place to absorb L_{out}, i.e., through the series inductor L [Fig. 1(c)].

IV. IMPLEMENTATION AND MEASUREMENT

To validate the theory and simulation results described in Sections II and III-C, we built two PA prototypes: one implemented with an IRF630 MOSFET and lumped elements at 1 MHz while the other implemented with a Cree CGH40010F GaN HEMT and TLs at 1.5 GHz.

A. Low-Frequency Implementation With Lumped Elements

A power MOSFET IRF630 with an intrinsic output capacitance of 200 pF is used in this design. The PA was designed at 1 MHz based on the topology in Fig. 1(c). Table III presents the load-network parameters extracted from Fig. 4 for two

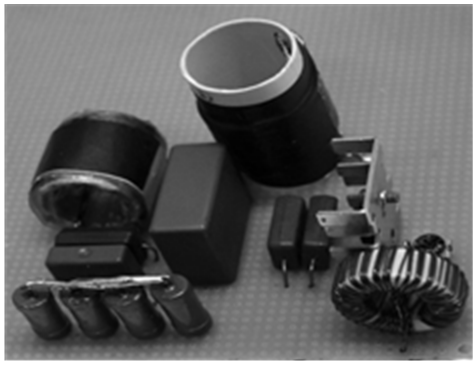

Fig. 8. Constructed PA prototype 1.

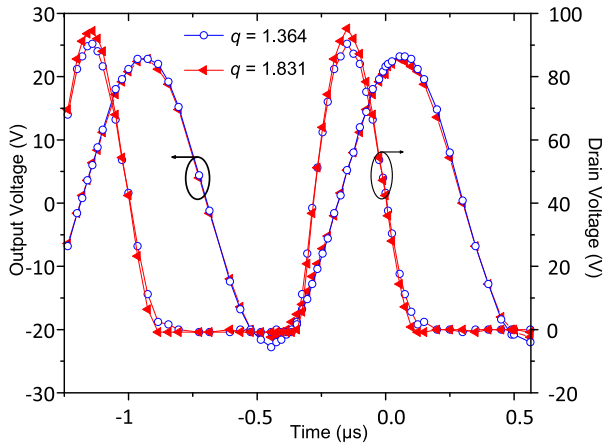

Fig. 9. Measured drain and output voltage waveforms of PA prototype 1. $q = 1.364$. $q = 1.831$.

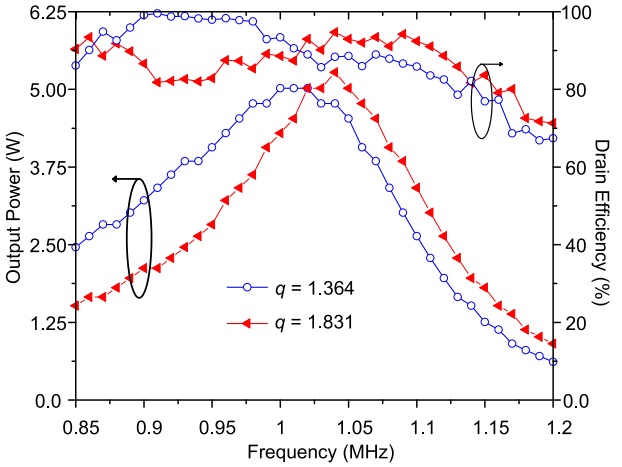

Fig. 10. Measured *DE* and output power of PA prototype 1. $q = 1.364$. $q = 1.831$.

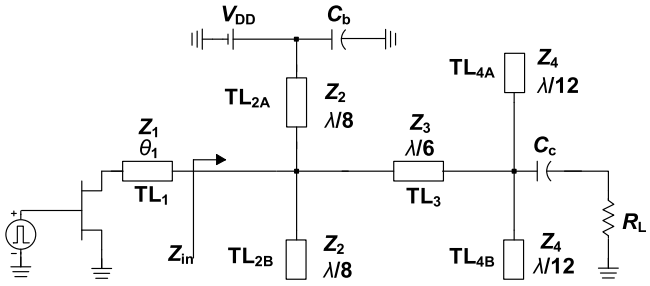

Fig. 11. Basic circuit schematic of PA prototype 2 using TLs.

arbitrary q values, i.e., 1.364 and 1.831 that results in a capacitive and inductive reactance X, respectively.

For a specified $V_{DD} = 24$ V and $P_{out} = 5$ W, the circuit component values were determined as: $C_x = 2.99$ nF, $L = 20.42$ μH, $C = 667.98$ pF, and $R = 55.99$ Ω for $q = 1.364$, and $L_x = 4.488$ μH, $L = 6.39$ μH, $C = 1.182$ nF, and $R = 39.168$ Ω for $q = 1.831$. The shunt filter was implemented for $Q_L = 5$, resulting in $L_0 = 1.57$ μH and $C_0 = 16.14$ nF.

The component values were slightly tuned to take into account the nonlinearity effect of the transistor output capacitance and parasitic ESR of the reactive components while preserving the nominal Class-E conditions.

Fig. 8 shows the photograph of the PA prototype 1, where the load is realized using four parallel connected 2-W resistors. Fig. 9 shows the measured drain and output voltage waveforms, with the former satisfying the ZVS and ZVDS conditions required for soft-switching and high-efficiency operation.

The measured PA performance in Fig. 10 shows that at 1 MHz, the PA delivered a *DE* of 93.3%, an output power (P_{out}) of 5 W for $q = 1.364$ and a *DE* of 88.6%, a P_{out} of 4.3 W for $q = 1.831$. The lower than-specified output power for $q = 1.831$ is mainly due to the parasitic ESR of the shunt L_0C_0 resonator [14].

B. High-Frequency Implementation With Transmission Lines

The second PA prototype was designed at 1.5 GHz as in Section III-C. The basic circuit schematic of the PA prototype 2 with a TL load-network is shown in Fig. 11, where C_c is a dc blocking capacitor and C_b is a bypass capacitor. The excess inductor L_e is realized using a series TL_1 with a characteristic impedance of Z_1 and electrical length of θ_1, whose value is determined using the following equation:

$$\theta_1 = \tan^{-1}\left(\frac{\omega_0 L_e}{Z_1}\right). \tag{15}$$

For θ_1 in (15) to be considered sufficiently short at f_0, the value of Z_1 should be selected to satisfy the relationship in the following equation:

$$Z_1 > \frac{4\omega_0 L_e}{\pi}. \tag{16}$$

A shorted $\lambda/8$ stub (TL_{2A}) together with an open-circuited $\lambda/8$ stub (TL_{2B}) with Z_2 set to a high value enforce a short-circuit termination at even harmonic frequencies and an open-circuit termination at fundamental and odd harmonic frequencies [15]. A series $\lambda/6$ TL_3 in conjunction with two open-circuited $\lambda/12$ stubs (TL_{4A} and TL_{4B}) enforce a short-circuit termination at $3f_0$. Hence, $Z_{in} = 0$ Ω at $2nf_0$ and $3f_0$, satisfying the load impedance requirement in Fig. 1(f). The characteristic impedances of TL_3 and TL_{4A}/TL_{4B}, i.e., Z_3 and Z_4, respectively, are calculated to match $Z_{opt} = (R + jX)$ Ω $= (25.1 + j20.4)$ Ω to the standard 50 Ω load resistance (R_L), thus satisfying the load impedance requirement in Fig. 1(e). At

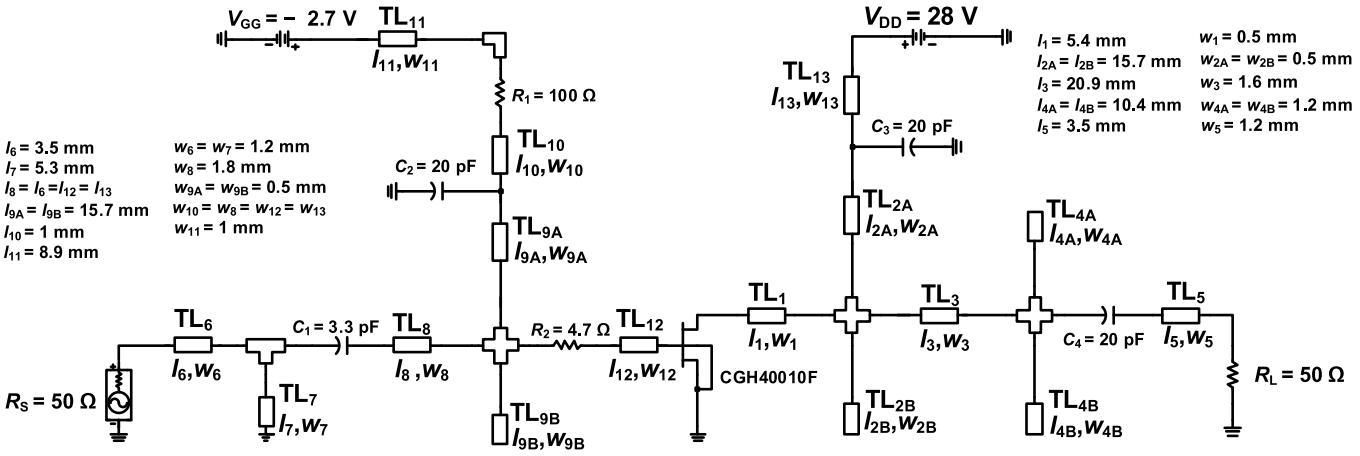

Fig. 12. Simulated circuit schematic of PA prototype 2.

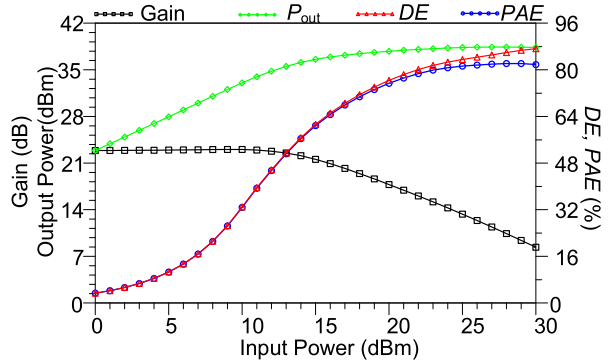

Fig. 13. Simulated PA performance versus input power at 1.5 GHz with $V_{DD} = 28$ V and $V_{GG} = -2.7$ V.

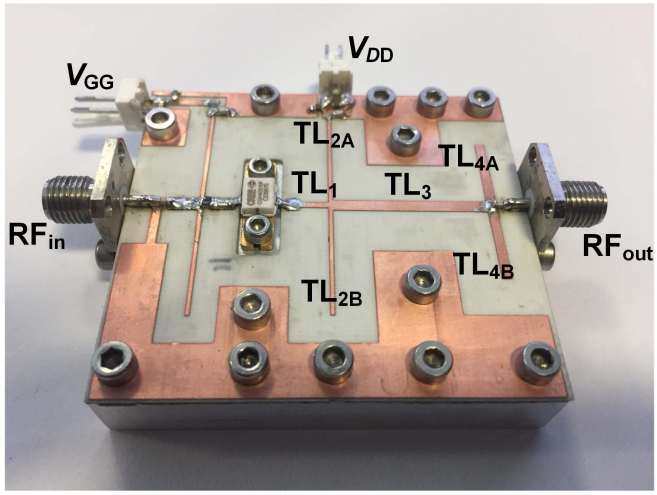

Fig. 14. Constructed PA prototype 2.

f_0, the input impedance Z_{in} is given by the following equation:

$$Z_{in} = Z_3 \left[\frac{3Z_3Z_4 + j\sqrt{3}(2Z_3 - Z_4)R_L}{(2Z_3 + 3Z_4)R_L - j\sqrt{3}Z_3Z_4} \right] \tag{17}$$

For R_L to be matched to Z_{opt} at f_0, $\mathrm{Re}\{Z_{in}\} = R$ and $\mathrm{Im}\{Z_{in}\} = X$, resulting in a system of two equations with two unknowns parameters described in (18) and (19), from which Z_3 and Z_4 are obtained as 50 and 63.5 Ω, respectively

$$3Z3^2Z4^2(4R_L - R) - R_L^2R(2Z_3 + 3Z_4)^2 = 0 \tag{18}$$

$$3Z_3^2Z_4^2\left(\sqrt{3}Z_3 - X\right) + R_L^2(2Z_3 + 3Z_4) \times\left[\sqrt{3}Z_3(2Z_3 - Z_4) - X(2Z_3 + 3Z_4)\right] = 0 \tag{19}$$

Harmonic-balance simulations were performed on the PA circuit depicted in Fig. 12 within the Keysight's Advanced Design System (ADS) environment. The simulation results in Fig. 13 show that the PA delivers a peak *DE* of 89.2%, a peak *PAE* of 83.7%, a peak P_{out} of 38.6 dBm, and a small-signal gain of 22.9 dB at 1.5 GHz.

The PA prototype 2 was constructed on a 0.51-mm-thick Rogers RO4003C substrate with a dielectric constant of 3.55 and a loss tangent of 0.0027, as shown in Fig. 14. A continuous-wave signal was applied to the PA using a Rohde & Schwarz SMR20 signal generator while the output power was measured by a Keysight's N9320A spectrum analyzer. A 40-dB attenuator was connected between the PA and the spectrum analyzer. The gate and drain biasing voltages were provided by a Thurlby 32-V dc power supply.

The measured PA performance in Fig. 15 shows that when biased with $V_{GG} = -2.7$ V and $V_{DD} = 28$ V, the PA delivers a peak *DE* of 90.2%, a peak *PAE* of 82.6%, a peak P_{out} of 39.8 dBm, and a linear gain of 14 dB at an operating frequency of 1.37 GHz. The values of P_{out} and power gain at the peak *PAE* are 39.6 dBm and 11.5 dB, respectively. The deviation between results in Figs. 13 and 15 is likely due to the fabrication tolerance and the inaccuracy of the transistor's large-signal model, for instance, in capturing the effect of the package parasitics.

Fig. 16 shows the measured output power, gain, *DE*, and *PAE* with the frequency swept from 1.32 to 1.5 GHz at an input power level of 28.3 dBm.

The PA delivers *DE* and *PAE* > 60%, $P_{out} = 38.6 \pm 1$ dBm, and power gain > 9.9 dB over the 180-MHz frequency range.

Fig. 17 shows the measured output power, gain, *DE*, and *PAE* with the drain supply voltage swept from 14 to 32 V at

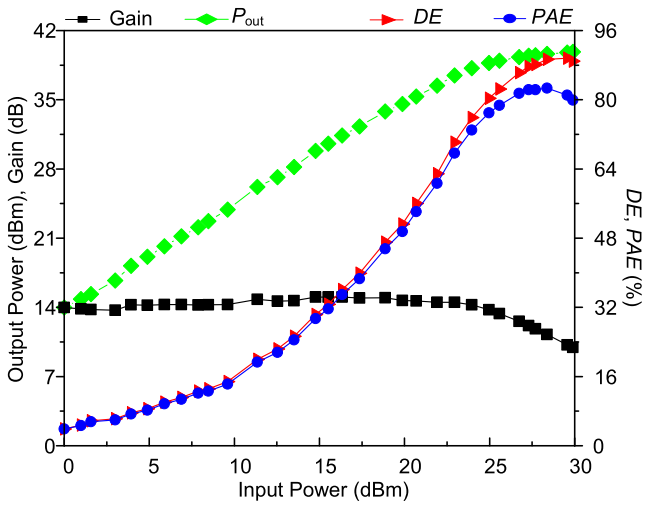

Fig. 15. Measured PA performance versus input power at 1.37 GHz with $V_{DD} = 28$ V and $V_{GG} = -2.7$ V.

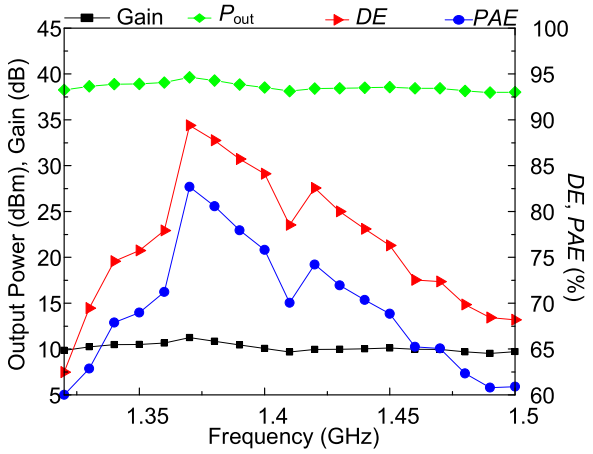

Fig. 16. Measured PA performance versus frequency at $P_{in} = 28.3$ dBm with $V_{DD} = 28$ V and $V_{GG} = -2.7$ V.

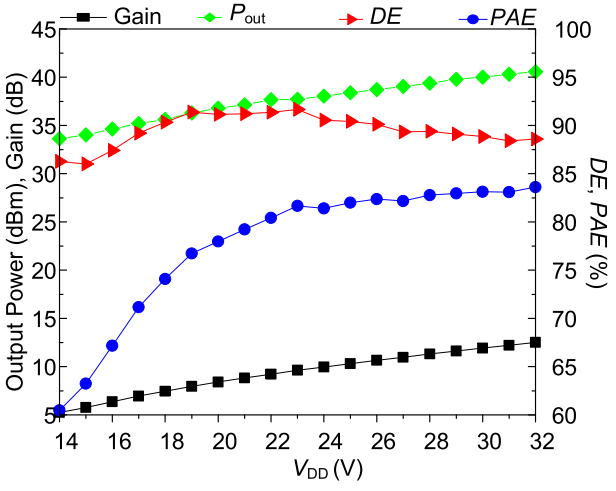

Fig. 17. Measured PA performance versus drain supply voltage at 1.37 GHz with $P_{in} = 28.3$ dBm and $V_{GG} = -2.7$ V.

an operating frequency of 1.37 GHz and an input power level of 28.3 dBm. The PA delivers a $DE > 85\%$ and a $PAE > 60\%$ over the specified range of V_{DD}, showing the potential

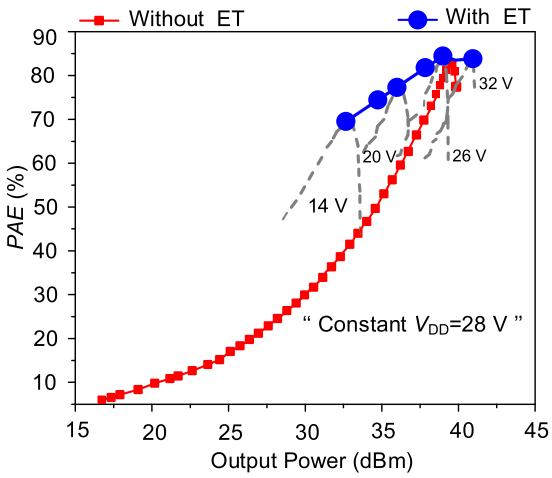

Fig. 18. Measured instantaneous *PAE* versus output power with quasi-static ET.

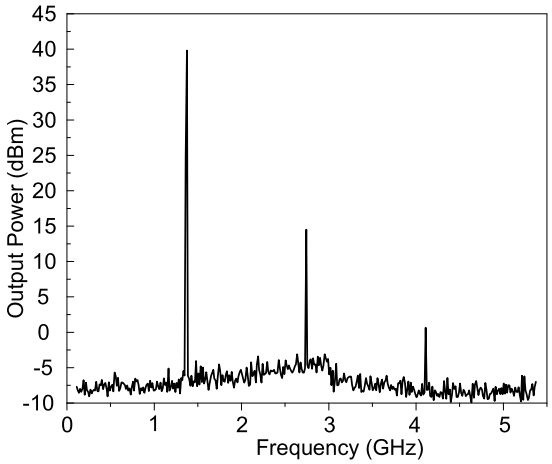

Fig. 19. Measured output power spectrum at $V_{DD} = 28$ V and $V_{GG} = -2.7$ V.

of operating the PA efficiently at lower drain supply voltages for deployment in polar transmitters or envelope elimination and restoration (EER) systems.

Fig. 18 shows the plot of the instantaneous *PAE* of the PA against output power for a constant $V_{DD} = 28$ V, from which it can be seen that the *PAE* degrades substantially as P_{out} decreases. It can also be seen that by operating the PA with reduced V_{DD} values at low P_{out}, the *PAE* can be greatly improved. Each dashed line in Fig. 18 is obtained by biasing the PA with a particular V_{DD} value while sweeping the input power.

The peaks of these lines are then joined and interpolated to establish a quasi-static envelope tracking (ET) curve. For example, the ET curve gives a *PAE* of 77.7% at P_{out} of 36.3 dBm. This is achieved by setting the V_{DD} and the input power to 20 V and 26.2 dBm. In contrast, to obtain the same level of output power, the constant "$V_{DD} = 28$ V" curve gives a much lower *PAE* of 59.5% at an input power of 22.48 dBm.

Fig. 19 shows the measured output power spectrum with the second and third harmonic suppression levels of 25 and 39.7 dBc, respectively, showing the effectiveness of the

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER GAN PAS

Ref	Freq (GHz)	V_{DD} (V)	P_{out} (dBm)	*DE* (%)	*PAE* (%)	Gain (dB)
[15]	2.22	28	39.5	91	80	9.2
[16]	2.8	28	40.1	77.5	70.8	10.7
[17]	1.5	28	42	85	81	13.1
[18]	2.14	30	40	76	73.1	14
[19]	3.5	26	40.2	75.8	70	12
This work	1.37	28	39.8	90.2	82.7	11.5

proposed TL load network. The PA performance is summarized in Table IV and compared with other pertinent work.

V. CONCLUSION

The theoretical analysis of a generalized Class-E PA with shunt capacitance and shunt filter with 50% duty ratio, including the explicit derivation of the idealized optimum voltage and current waveforms and load-network parameters has been presented and verified through frequency-domain simulations and experiments. The calculated and simulated switch voltage and current waveforms show good agreement between them while fulfilling the ZVS and ZVDS conditions of the Class-E operation. Two PA prototypes, i.e., one designed with lumped elements at low frequency and the other designed with TLs at high frequency, have been built and measured, with both PAs achieving a peak *DE* of around 90% and excellent second and third harmonic suppression levels.

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