Harmonic Termination Effects on the Performance of 39-GHz Stacked CMOS Power Amplifiers


Published in:
IEEE Asia-Pacific Microwave Conference (APMC), Singapore

Document Version:
Peer reviewed version

Queen's University Belfast - Research Portal:
Link to publication record in Queen's University Belfast Research Portal

Publisher rights
Copyright 2019 IEEE. This work is made available online in accordance with the publisher's policies. Please refer to any applicable terms of use of the publisher.

General rights
Copyright for the publications made accessible via the Queen's University Belfast Research Portal is retained by the author(s) and / or other copyright owners and it is a condition of accessing these publications that users recognise and abide by the legal requirements associated with these rights.

Take down policy
The Research Portal is Queen's institutional repository that provides access to Queen's research output. Every effort has been made to ensure that content in the Research Portal does not infringe any person’s rights, or applicable UK laws. If you discover content in the Research Portal that you believe breaches copyright or violates any law, please contact openaccess@qub.ac.uk.

Open Access
This research has been made openly available by Queen's academics and its Open Research team. We would love to hear how access to this research benefits you. – Share your feedback with us: http://go.qub.ac.uk/oa-feedback
Harmonic Termination Effects on the Performance of 39-GHz Stacked CMOS Power Amplifiers

Matthew Love  
*Queen’s University of Belfast*  
Northern Ireland  
mlove05@qub.ac.uk

Mury Thian  
*Queen’s University of Belfast*  
Northern Ireland  
m.thian@qub.ac.uk

Floris van der Wilt  
*Catena Microelectronics B.V.*  
The Netherlands

Koen van Hartingsveldt  
*Catena Microelectronics B.V.*  
The Netherlands

Kave Kianush  
*Catena Microelectronics B.V.*  
The Netherlands

Abstract—The effects of the second and third harmonic impedances, $Z_{2f_0}$ and $Z_{3f_0}$, on the performance of millimeter-wave power amplifiers (PA) designed on the GlobalFoundries 22FDX CMOS process are investigated in this paper. Two sets of load-pull simulations, one with ideal drain bias-tee and another with non-ideal circuitry included, show that terminating the harmonics with open-circuits increases the efficiency while terminating them with short-circuits decreases it. The effects on the performance are much larger for the second harmonic termination than for the third. Four circuits were designed to evaluate all four combinations of open/short circuit harmonic terminations. The circuit with $Z_{2f_0} = \infty$ and $Z_{3f_0} = 0$ had the highest performance with PAE of 38.3%, $P_{out}$ of 19 dBm, and $P_{out} -3$ dB BW of 20.3 GHz. The remaining three circuits had less competitive performance due to their more complicated load networks and higher output matching transformation ratios.

Index Terms—22 nm, 5G NR, CMOS, efficiency, integrated circuit, Ka-band, millimeter wave, power amplifier

I. INTRODUCTION

The 5G standard has resulted in significant attention in millimeter wave (mmW) power amplifier (PA) design in the 28 GHz and 39 GHz bands [1], [2]. There is high interest in CMOS PAs as CMOS allows total integration of digital/analog/RF circuitry on the same die. Modern nanoscale CMOS processes with oscillation frequencies ($f_{\text{max}}$) exceeding 350 GHz are viable for mmW PA design and output powers of 9-16 dBm, specified for 5G NR, can be readily achieved [3]. The high DC power consumption of PAs makes optimizing their efficiency a high priority. One technique is to terminate the harmonic-frequency components with open and short circuits to shape the drain voltage and current waveforms to reduce current-voltage overlap across the transistors. In this paper, the effects that different harmonic terminations have on the mmW CMOS PA performance in terms of efficiency and output power will be investigated for the first time. Four PAs with the second and third harmonics terminated with combinations of open and short circuits were designed at a center frequency of 39 GHz on the GlobalFoundries 22 nm FD-SOI CMOS process. The amplifiers are named $A_{x,y}$ with $x$ and $y$ being the 2$f_0$ and 3$f_0$ termination impedances respectively, e.g., $A_{o,s}$ has an open circuit to 2$f_0$ and short circuit to 3$f_0$. Higher harmonics aren’t considered as they have negligible effects. The results are then compared with a reference amplifier with no harmonic terminations $A_{rr}$.

II. CIRCUIT DESIGN AND DESCRIPTION

The circuits use the triple-stacked architecture in Fig. 1 to allow the use of a 3 V supply voltage [4]. Using a single common-source stage requires wider transistors leading to lower efficiency as the lower optimal impedance incurs greater matching losses and the larger capacitive parasitics reduce $f_{\text{max}}$. A triple-stack architecture provides a compromise between output power ($P_{out}$) and efficiency as the transistor turn-on delays limit the total realizable drain voltage swing. The transistors $M_1$-$M_3$ are 148.5 $\mu$m wide, 17 $\mu$m long, and

![Fig. 1. Triple-stacked PA architecture with an ideal bias tee ($L_b$ and $C_b$) and a load tuner used in the initial load-pull simulations](image)

<table>
<thead>
<tr>
<th>Amp</th>
<th>PAE (%)</th>
<th>$P_{out}$ (dBm)</th>
<th>$Z_{\text{opt}}$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{rr}$</td>
<td>52.9</td>
<td>17.8</td>
<td>17.3 + j35.4</td>
</tr>
<tr>
<td>$A_{o,s}$</td>
<td>55.7</td>
<td>18.3</td>
<td>16.2 + j30.4</td>
</tr>
<tr>
<td>$A_{o,o}$</td>
<td>56.2</td>
<td>18.3</td>
<td>16.2 + j30.4</td>
</tr>
<tr>
<td>$A_{s,o}$</td>
<td>50.5</td>
<td>18.3</td>
<td>21.6 + j25.1</td>
</tr>
<tr>
<td>$A_{s,s}$</td>
<td>48.2</td>
<td>18.1</td>
<td>23.4 + j25.7</td>
</tr>
</tbody>
</table>

This work was supported by the UK Engineering and Physical Sciences Research Council (EPSRC) under grant no. EP/P013031/1.
the trends in the previous simulations (Table I) remain true. As can be seen from Table II, the circuits see a predictable drop in performance due to more accurate values for $Z_{\text{ind}}$ and harmonic terminations, hence resulting in to take into account the effects of non-ideal finite dc-feed inductances and harmonic circuitry can have on $Z_{\text{opt}}$. The optimum fundamental-frequency impedance $Z_{\text{opt}}$ is strongly affected by the $2f_0$ impedance ($Z_{2f_0}$) while the $3f_0$ impedance ($Z_{3f_0}$) has a much smaller effect. The second set of load-pull simulations, shown in Fig. 2(a)-(d), replace the ideal bias tee used in the initial load-pull with some components using foundry models to take into account the effects of non-ideal finite dc-feed inductances and harmonic terminations, hence resulting in more accurate values for $Z_{\text{opt}}$. As can be seen from Table II, the circuits see a predictable drop in performance due to the parasitic resistance of the non-ideal components though the trends in the previous simulations (Table I) remain true with $A_{oo}$ having the best performance. The use of non-ideal components results in a much larger variation in $Z_{\text{opt}}$ with the $A_{oo}$ and $A_{oo}$ circuits seeing an increase in $Z_{\text{opt}}$ whereas the $A_{oo}$ circuit sees a decrease in $Z_{\text{opt}}$. The second set of load-pull simulations show the drastic effect that non-ideal finite dc-feed inductances and harmonic circuitry can have on $Z_{\text{opt}}$ and thus it is encouraged to include as many non-ideal components as possible in the load-pull simulations to get the most accurate value for $Z_{\text{opt}}$. The final load networks including the output matching and harmonic termination circuitries are shown in Fig. 3(a)-(d) with component values given in Table III. Circuits with short-circuited harmonics require more components as possible in the load-pull simulations to get the most accurate value for $Z_{\text{opt}}$. As can be seen from Table II, the circuits see a predictable drop in performance due to the parasitic resistance of the non-ideal components though the trends in the previous simulations (Table I) remain true with $A_{oo}$ having the best performance. The use of non-ideal components results in a much larger variation in $Z_{\text{opt}}$ with the $A_{oo}$ and $A_{oo}$ circuits seeing an increase in $Z_{\text{opt}}$ whereas the $A_{oo}$ circuit sees a decrease in $Z_{\text{opt}}$. The second set of load-pull simulations show the drastic effect that non-ideal finite dc-feed inductances and harmonic circuitry can have on $Z_{\text{opt}}$ and thus it is encouraged to include as many non-ideal components as possible in the load-pull simulations to get the most accurate value for $Z_{\text{opt}}$. Table III. Component values

<table>
<thead>
<tr>
<th>Circuit</th>
<th>$PAE$ (%)</th>
<th>$P_{\text{out}}$ (dBm)</th>
<th>$Z_{\text{opt}}$ (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{oo}$</td>
<td>46.4</td>
<td>18</td>
<td>57.1 + j20.6</td>
</tr>
<tr>
<td>$A_{oo}$</td>
<td>52.6</td>
<td>18.1</td>
<td>33.9 + j36.8</td>
</tr>
<tr>
<td>$A_{so}$</td>
<td>44.8</td>
<td>17.9</td>
<td>21.7 + j25.5</td>
</tr>
<tr>
<td>$A_{ss}$</td>
<td>41.6</td>
<td>17.8</td>
<td>16.6 + j22.9</td>
</tr>
</tbody>
</table>

Resistances in kΩ, capacitances in fF, Inductances in pH

![Fig. 2. Improved load-pull setup for (a) $A_{oo}$, (b) $A_{oo}$, (c) $A_{so}$, and (d) $A_{ss}$. All components use non-ideal foundry models except for $C_B$ which is an ideal dc blocking capacitor.](image1)

![Fig. 3. Final load networks for (a) $A_{oo}$, (b) $A_{oo}$, (c) $A_{so}$, and (d) $A_{ss}$. The green, red, and blue regions are resonating at $f_0$, $2f_0$, and $3f_0$ respectively.](image2)
some state-of-the-art circuits. The $PAE$ and $P_{\text{out}}$ are plotted versus frequency in Fig. 4 from 25 GHz to 55 GHz. Circuit $A_{\text{os}}$ has the best performance of the four circuits in terms of $PAE$, $P_{\text{out}}$, gain, and 3 dB bandwidth while offering excellent second and third harmonic suppression levels. The bandwidth of $A_{\text{os}}$ is wide enough to amplify signals in the 28 GHz band, in addition to the 39 GHz band, with $P_{\text{out}}$ of 15 dBm at 28 GHz. $A_{\text{oo}}$ has a simpler circuit than $A_{\text{os}}$, with one fewer inductor, though at the cost of slightly lower performance (except the 3$f_0$ attenuation which is considerably better). The $A_{\text{so}}$ and $A_{\text{ss}}$ circuits have the lowest performance, as indicated by the load-pull simulations though the harmonic suppression is arguably better overall. The lower performance of $A_{\text{so}}$ compared with $A_{\text{os}}$, contrary to the load-pull simulations, is due to the larger output matching transformation ratio which increased the matching losses. When compared with [5]–[8], $A_{\text{os}}$ provides good competition in terms of $PAE$, $P_{\text{out}}$, and 3 dB BW.

### IV. Conclusion

The effects of the second and third harmonic terminations on the performance of mmW PAs designed in a 22 nm FDSOI CMOS process have been investigated. Two load-pull simulations, one with an ideal bias tee and another with non-ideal components, indicate that providing open-circuit terminations to the harmonics increases the PA efficiency while presenting short-circuits reduces it. Simulation results of the complete circuits show the best performing circuit to be the version with the second harmonic terminated with an open-circuit and the third-harmonic with a short circuit. It has excellent $PAE$, $P_{\text{out}}$, and 3 dB bandwidth when compared with the state of the art. The slightly lower performance of the PA with both harmonics terminated with open-circuits is attributed to the larger output matching transformation ratio that led to higher matching losses.

**REFERENCES**


