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Harmonic Termination Effects on the Performance of 39-GHz Stacked CMOS Power Amplifiers

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Abstract—The effects of the second and third harmonic impedances, Z_{2f_0} and Z_{3f_0} , on the performance of millimeter-wave power amplifiers (PA) designed on the GlobalFoundries 22FDX CMOS process are investigated in this paper. Two sets of load-pull simulations, one with ideal drain bias-tee and another with non-ideal circuitry included, show that terminating the harmonics with open-circuits increases the efficiency while terminating them with short-circuits decreases it. The effects on the performance are much larger for the second harmonic termination than for the third. Four circuits were designed to evaluate all four combinations of open/short circuit harmonic terminations. The circuit with $Z_{2f_0} = \infty$ and $Z_{3f_0} = 0$ had the highest performance with PAE of 38.3%, P_{out} of 19 dBm, and P_{out} -3 dB BW of 20.3 GHz. The remaining three circuits had less competitive performance due to their more complicated load networks and higher output matching transformation ratios.

Index Terms—22 nm, 5G NR, CMOS, efficiency, integrated circuit, Ka-band, millimeter wave, power amplifier

I. INTRODUCTION

The 5G standard has resulted in significant attention in millimeter wave (mmW) power amplifier (PA) design in the 28 GHz and 39 GHz bands [1], [2]. There is high interest in CMOS PAs as CMOS allows total integration of digital/analog/RF circuitry on the same die. Modern nanoscale CMOS processes with oscillation frequencies (f_{max}) exceeding 350 GHz are viable for mmW PA design and output powers of 9-16 dBm, specified for 5G NR, can be readily achieved [3]. The high DC power consumption of PAs makes optimizing their efficiency a high priority. One technique is to terminate the harmonic-frequency components with open and short circuits to shape the drain voltage and current waveforms to reduce current-voltage overlap across the transistors. In this paper, the effects that different harmonic terminations have on the mmW CMOS PA performance in terms of efficiency and output power will be investigated for the first time. Four PAs with the second and third harmonics terminated with combinations of open and short circuits were designed at a center frequency of 39 GHz on the GlobalFoundries 22 nm FDSOI CMOS process. The amplifiers are named A_{xy} with x and y being the $2f_0$ and $3f_0$ termination impedances

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Fig. 1. Triple-stacked PA architecture with an ideal bias tee (L_b and C_b) and a load tuner used in the initial load-pull simulations

TABLE I
INITIAL LOAD-PULL SETUP (FIG. 1)

Amp	PAE (%)	P_{out} (dBm)	Z_{opt} (Ω)
A_{rr}	52.9	17.8	$17.3 + j35.4$
A_{os}	55.7	18.3	$16.2 + j30.4$
A_{oo}	56.2	18.3	$16.2 + j30.4$
A_{so}	50.5	18.3	$21.6 + j25.1$
A_{ss}	48.2	18.1	$23.4 + j25.7$

respectively, e.g., A_{os} has an open circuit to $2f_0$ and short circuit to $3f_0$. Higher harmonics aren't considered as they have negligible effects. The results are then compared with a reference amplifier with no harmonic terminations A_{rr} .

II. CIRCUIT DESIGN AND DESCRIPTION

The circuits use the triple-stacked architecture in Fig. 1 to allow the use of a 3 V supply voltage [4]. Using a single common-source stage requires wider transistors leading to lower efficiency as the lower optimal impedance incurs greater matching losses and the larger capacitive parasitics reduce f_{max} . A triple-stack architecture provides a compromise between output power (P_{out}) and efficiency as the transistor turn-on delays limit the total realizable drain voltage swing. The transistors M_1 - M_3 are $148.5 \mu\text{m}$ wide, 17 nm long, and

Fig. 2. Improved load-pull setup for (a) A_{os} , (b) A_{oo} , (c) A_{so} , and (d) A_{ss} . All components use non-ideal foundry models except for C_B which is an ideal dc blocking capacitor. The green, red, and blue regions are resonating at f_0 , $2f_0$, and $3f_0$ respectively.

TABLE II
IMPROVED LOAD-PULL SETUP (FIG. 2)

Circuit	PAE (%)	P_{out} (dBm)	Z_{opt} (Ω)
A_{os}	46.4	18	$57.1 + j20.6$
A_{oo}	52.6	18.1	$33.9 + j36.8$
A_{so}	44.8	17.9	$21.7 + j25.5$
A_{ss}	41.6	17.8	$16.6 + j22.9$

are optimized for mmW performance with an undoped backgate to reduce channel-to-substrate capacitances. The inductors and transmission lines are implemented on the two top metals (2800 nm thick aluminum and 2700 nm thick copper respectively) and the capacitors on the bottom seven metal layers (80 nm–90 nm thick copper).

Two different load-pull simulations were performed to evaluate the effects of the harmonic terminations. The first set of load-pull simulations shown in Fig. 1 use an ideal bias-tee in conjunction with a load tuner, which sets the harmonic impedances (open/short circuits), to illustrate the maximum achievable PA performance independent of implementation details. The results, summarized in Table I, show that open-circuit terminations increase the power-added efficiency (PAE) with P_{out} being relatively unaffected, while short-circuit terminations reduce the PAE. The optimum fundamental-frequency impedance Z_{opt} is strongly affected by the $2f_0$ impedance (Z_{2f_0}) while the $3f_0$ impedance (Z_{3f_0}) has a much smaller effect. The second set of load-pull simulations, shown in Fig. 2(a)-(d), replace the ideal bias tee used in the initial load-pull with some components using foundry models to take into account the effects of non-ideal finite dc-feed inductances and harmonic terminations, hence resulting in more accurate values for Z_{opt} . As can be seen from Table II, the circuits see a predictable drop in performance due to the parasitic resistance of the non-ideal components though the trends in the previous simulations (Table I) remain true

Fig. 3. Final load networks for (a) A_{os} , (b) A_{oo} , (c) A_{so} , and (d) A_{ss} . The green, red, and blue regions are resonating at f_0 , $2f_0$, and $3f_0$ respectively.

TABLE III
COMPONENT VALUES

A_{os}	A_{oo}	A_{so}	A_{ss}
$R_1 = 12$	$R_1 = 12$	$R_1 = 12$	$R_1 = 12$
$R_2 = 12$	$R_2 = 12$	$R_2 = 12$	$R_2 = 12$
$C_1 = 4.2 \text{ k}$	$C_1 = 500$	$C_1 = 1 \text{ k}$	$C_1 = 1 \text{ k}$
$C_2 = 198$	$C_2 = 53$	$C_2 = 112$	$C_2 = 111$
$C_3 = 15$	$C_3 = 55$	$C_3 = 82$	$C_3 = 80$
$C_4 = 83$	$C_4 = 55$	$C_4 = 93$	$C_4 = 277$
$C_5 = 29$	$L_1 = 343$	$L_1 = 405$	$L_1 = 163$
$L_1 = 187$	$L_2 = 546$		$L_2 = 126$
$L_2 = 149$			
$L_3 = 319$			

Resistances in k Ω , capacitances in fF, Inductances in pH

with A_{oo} having the best performance. The use of non-ideal components results in a much larger variation in Z_{opt} with the A_{os} and A_{oo} circuits seeing an increase in Z_{opt} whereas the A_{ss} circuit sees a decrease in Z_{opt} . The second set of load-pull simulations show the drastic effect that non-ideal finite dc-feed inductances and harmonic circuitry can have on Z_{opt} and thus it is encouraged to include as many non-ideal components as possible in the load-pull simulations to get the most accurate value for Z_{opt} . The final load networks including the output matching and harmonic termination circuitries are shown in Fig. 3(a)-(d) with component values given in Table III. Circuits with short-circuited harmonics require more components with A_{ss} requiring six while A_{oo} only needs four. The gate capacitances of some circuits are slightly tuned from the original load-pull values in Fig. 1 to reduce the peak drain-source voltage of some of the transistors.

III. RESULTS

The triple-stacked PA circuit in Fig. 1 in conjunction with the load networks in Fig. 3 were simulated in Cadence SpectreRF using experimentally validated mmW foundry models. The results are summarized in Table IV and compared with

TABLE IV
PA PERFORMANCE COMPARED WITH THE STATE OF THE ART

Ref.	Process	Freq. (GHz)	PAE (%)	P_{out} @ f_0 (dBm)	P_{out} @ $2f_0$ (dBm)	P_{out} @ $3f_0$ (dBm)	Gain (dB)	BW ⁺ _{-3 dB} (GHz)	Supply (V)	Architecture
A_{os} [#]	22 nm FDSOI CMOS	39	38.3	19	-18	-17.3	13	20.3	3	Triple Stacked
A_{oo} [#]	22 nm FDSOI CMOS	39	34.2	17.9	-13.4	-33.8	11.9	11.9	3	Triple Stacked
A_{so} [#]	22 nm FDSOI CMOS	39	31.3	17.8	-35	-28	11.8	11.1	3	Triple Stacked
A_{ss} [#]	22 nm FDSOI CMOS	39	29.8	17.4	-22.6	-17.4	11.4	13	3	Triple Stacked
[5]	65 nm Bulk CMOS	32	32.9	12.9	N/A	N/A	20.8	20.2	1	Differential CS
[6]	65 nm Bulk CMOS	39	31.2	17.2	N/A	N/A	17	5	1.1	Differential CS
[7]	28 nm Bulk CMOS	34	24.2	16.6	N/A	N/A	20.8	28	0.9	Differential + Combiner
[8]	130 nm SiGe	39	21.4	17.1	N/A	N/A	16.6	> 16	1.5	Differential + Combiner

[#] Simulated using experimentally validated mmW foundry models, $P_{in} = 6$ dBm

⁺ P_{out} -3 dB bandwidth

some state-of-the-art circuits. The PAE and P_{out} are plotted versus frequency in Fig. 4 from 25 GHz to 55 GHz. Circuit A_{os} has the best performance of the four circuits in terms of PAE , P_{out} , gain, and 3 dB bandwidth while offering excellent second and third harmonic suppression levels. The bandwidth of A_{os} is wide enough to amplify signals in the 28 GHz band, in addition to the 39 GHz band, with P_{out} of 15 dBm at 28 GHz. A_{oo} has a simpler circuit than A_{os} , with one fewer inductor, though at the cost of slightly lower performance (except the $3f_0$ attenuation which is considerably better). The A_{so} and A_{ss} circuits have the lowest performance, as indicated by the load-pull simulations though the harmonic suppression is arguably better overall. The lower performance of A_{oo} compared with A_{os} , contrary to the load-pull simulations, is due to the larger output matching transformation ratio which increased the matching losses. When compared with [5]–[8], A_{os} provides good competition in terms of PAE , P_{out} , and 3 dB BW.

IV. CONCLUSION

The effects of the second and third harmonic terminations on the performance of mmW PAs designed in a 22 nm FDSOI CMOS process have been investigated. Two load-pull simulations, one with an ideal bias tee and another with non-ideal components, indicate that providing open-circuit terminations to the harmonics increases the PA efficiency while presenting short-circuits reduces it. Simulation results of the complete circuits show the best performing circuit to be the version with the second harmonic terminated with an open-circuit and the third-harmonic with a short circuit. It has excellent PAE , P_{out} , and 3 dB bandwidth when compared with the state of the art. The slightly lower performance of the PA with both harmonics terminated with open-circuits is attributed to the larger output matching transformation ratio that led to higher matching losses.

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Fig. 4. PAE and P_{out} across frequency for $P_{in} = 6$ dBm. The circles and triangles lines represent PAE and P_{out} respectively for A_{os} (black), A_{oo} (red), A_{so} (blue), and A_{ss} (green).

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