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Low-Voltage Domain-Wall LiNbO₃ Memristors

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Abstract: Application of conducting ferroelectric domain walls (DW) as functional elements may facilitate development of conceptually new resistive switching devices. In a conventional approach, several orders of magnitude change in resistance can be achieved by controlling the DWs density using super-coercive voltage. However, a deleterious characteristic of this approach is high-energy cost of polarization reversal due to high leakage current. Here, we demonstrate a new approach based on tuning the conductivity of DWs themselves rather than on domain rearrangement. Using LiNbO₃ capacitors with graphene, we show that resistance of a device set to a polydomain state can be continuously tuned by application of sub-coercive voltage. The tuning mechanism is based on the reversible transition between the conducting and insulating states of DWs. The developed approach allows an energy-efficient control of resistance without the need for domain structure modification. The developed memristive devices are promising for multi-level memories and neuromorphic computing applications.

Keywords: lithium niobate, ferroelectric, conducting domain walls, memristor

Domain walls (DWs) in ferroelectrics exhibit physical properties that are completely different from the domains that they delineate.¹⁻⁶ Deployment of these properties coupled with electrical, mechanical and optical control of DW geometry, position and density ⁷ paves the way for development of highly scalable electronic devices with enhanced functionality. For example, conducting DWs observed in a number of ferroelectric materials ^{1,2,8-15} could be used in resistive memory devices where the low resistance state was induced by DWs writing and high resistance by their erasure. Experimental realization of this concept has been reported first using the BiFeO₃ thin films.^{16,17} A recently demonstrated functional domain wall-mediated memristor based on thin film LiNbO₃ (LNO) capacitors exhibits up to twelve orders of magnitude variation in resistance caused by the injection of strongly inclined conducting DWs.¹⁸ However, due to a high coercive field of LNO, this approach requires high voltages for DW injection or annihilation limiting its application in low-power devices. Also, once the device is set to the ON state by creating a polydomain structure, further modification would require even a higher energy input due the strong leakage current associated with the presence of conducting DWs.

Another approach to resistance modulation relies upon the change in conductance of the DWs themselves. In the earlier studies on conducting 180° DWs in bulk LNO, ¹⁹ it was reported that their conductivity could be tuned by manipulating the DW inclination angle with respect to the polar axis. Our recent findings show that the DW inclination angle in the LNO thin films can be increased up to 20° by an external bias resulting in significant enhancement of the DW conductivity.²⁰ A significant advantage of this approach is its energy efficiency as it does not require any substantial change in domain

configuration, hence the resistance modulation can be realized at the voltage level well below the coercive bias. In addition, it allows higher accuracy and reproducibility in programming the resistance states.

Here, we demonstrate and compare the use of both approaches in actual device geometry: the LNO-based memristor with parallel-plate capacitor configuration. We show that partial switching of polarization by application of super-coercive bias allows a change in capacitor resistance by four orders of magnitude due to generation of strongly inclined conducting 180° DWs. A direct correlation between the DW perimeter length and the device resistance is unambiguously established by monitoring the field-induced domain structure evolution and corresponding changes in I-V characteristics. Somewhat smaller but more reproducible modulation of resistance can be achieved by application of sub-coercive bias to the capacitor in the polydomain state due to the change in the DW conductance without polarization reversal. Pulse amplitude and duration serve as the variable parameters in both cases allowing realization of distinct resistance states.

The memristive device, investigated in this work, consists of the 500-nm-thick z-cut LNO film prepared by the ion-sliced method ²¹ on the Pt-coated bulk LNO substrate and multi-layer graphene (Gr) with the thickness of ~20 nm used as a top electrode, yielding a Gr/LNO/Pt parallel plate capacitor. Our previous studies have shown that graphene is an efficient top electrode material, which allows domain switching and imaging by piezoresponse force microscopy (PFM).^{22,23} Exceptional chemical, mechanical and thermal stability of graphene combined with its high electrical conductivity and low reactivity makes it an attractive top electrode material for the proposed memristive devices. We intentionally used relatively thick multi-layer graphene

stacks to ensure their stability during high-voltage polarization switching accompanied by a drastic change in device conductance. Indeed, graphene proved to be more robust than metal or oxide electrodes, which got burned or delaminated by high-density currents (see Figure S1).

It has been previously shown that interfacial molecular layers could strongly affect properties of devices based on a combination of two-dimensional and ferroelectric materials.^{22,23,24} To achieve well-controlled interfaces between graphene and LNO, the Gr/LNO/Pt structures were fabricated inside a nitrogen-filled glovebox. Prior to the deposition, the LNO surface was cleaned by n-hexane solution. A graphite crystal was exfoliated using an adhesive tape, which was pressed onto a LNO surface leaving graphene flakes that could be identified by optical microscopy. In the as-prepared LNO films, the polarization points away from the bottom electrode in the z^+ , or upward, direction. PFM imaging of domain structure and conductive atomic force microscopy (CAFM) testing of the resistive behavior were carried out with Pt-coated Si tips (PPP-EFM, Nanosensors) using a commercial AFM system (MFP-3D, Asylum Research).²⁰ In this paper, all switching voltages are given with respect to the top electrode.

Preliminary tests of the bare LNO film reveal a conducting behavior of the 180° DWs created by scanning the film surface with an electrically biased PFM tip. **Figures 1a** and **1b** show PFM and corresponding CAFM images of a series of the periodical stripe domains written by +60 V dc bias where, in agreement with the earlier reports, a strong current signal stems from the DWs only.¹⁵ PFM switching spectroscopy (**Fig. 1c**) yields a strongly shifted hysteresis loop with the coercive voltages of 32 V and -8 V resulting from asymmetric boundary conditions at the top and bottom interfaces.

Transmission electron microscopy (TEM) of the sample cross-section (**Fig. 1d**) displays strongly inclined head-to-head DWs with the inclination angle in the range of 10~16°, suggesting that these DWs are charged due to polarization discontinuity.

After preliminary testing, the domain structure evolution and the associated changes in the I-V characteristics as a function of applied voltage have been studied in the Gr/LNO/Pt memristor. A graphene flake of several square micrometers in size on top of the LNO film (**Fig. 2a**) has been used for electrical biasing of the device. As expected, application of the super-coercive voltage pulse of +33 V to the device initially in the single-domain state results in the formation of the poly-domain structure in an entire area covered by graphene (**Figs. 2b** and **2c**). Higher magnification PFM imaging in **Figs. 2,d-i** illustrates a gradual change in the domain configuration upon increase in the switching pulse amplitude. Domain nucleation initiated by the +31 V pulse (**Fig. 2d**) is followed by the nuclei lateral expansion at +32 V (**Fig. 2e**) and coalescence at +33 V and +34 V resulting in the formation of a maze structure (**Figs. 2f** and **2g**). Further voltage increase leads to domain merging through annihilation of the DWs and formation of a single-domain state with the downward polarization direction (**Figs. 2h**). This process is completely reversible as application of the -10 V voltage pulse switched the device back to the upward polarization (**Fig. 2i**).

The I-V characteristics of the Gr/LNO/Pt device have been measured for every domain state shown in **Figs. 2,d-h**. For the pristine state where the whole LNO volume is polarized upward, these measurements yield a current level as low as 0.2 pA (close to the noise level) (**Fig. 3a**). As soon as the poly-domain is created by the voltage pulse, the amount of current increases dramatically, from 20 pA for the +31 V up to 1 nA for the

+33 V pulse (**Fig. 3a**). Comparison of this behavior with the corresponding changes in the domain structure in **Fig. 2** allows us to attribute the current increase to the increasing length of the conductive DWs perimeter in the LNO film. Specifically, using image analysis of the PFM data in **Fig. 2**, we have extracted quantitative information related to domain configuration and plotted the device conductance as a function of the DW perimeter (**Fig. 3b**). A decrease of the current signal for the +37 V pulse, that drives the device to the downward-oriented single-domain state, is due to the erasure of the DWs in the device interior. The remaining DWs along the edges of the graphene flake (as is mentioned above, the pristine LNO film is in the upward polarization state) explains the finite conductivity of the device completely switched downward. Thus, DW-based memristive devices with the OFF/ON resistance ratio of at least 4 orders of magnitude can be realized in the Gr/LNO/Pt capacitors by employing the control of domain structure by super-coercive voltage.

An alternative approach to resistance modulation involves tuning of the DW conductivity rather than changing the domain configuration. As shown in **Figs. 4a** and **4b**, the device conductance can be tuned by application of the sub-coercive set voltage pulses when the device is in the poly-domain state. **Figure 4a** illustrates a dependence of the device conductance on the set pulse amplitude acquired after the poly-domain state was generated by application of the +33 V switching pulse. The set pulse amplitudes (in the range from -3 V to 8 V) are much lower than the coercive voltages, so that the domain structure stays almost intact (there is only a small DW displacement as explained below) while the resistance changes. It can be seen that varying a set pulse amplitude would change the device conductance by ~1-2 orders of magnitude and that this process

is reproducible. More specifically, an increase in the positive set pulse amplitude will lead to higher conductance, while a negative set pulse would decrease the device conductance. The device conductance could also be modified by varying the set pulse duration (**Fig. 4b**).

Since the domain structure is not affected by the sub-coercive set pulses, the tuning of device resistance must come from the modulation of DW conductance. This effect has been reported in our previous study on the LNO films without a top electrode and has been attributed to the electrically induced DW bending near the sample surface confirmed by cross-sectional STEM.²⁰ Specifically, bending the wall away from the polar direction makes it more conducting, while aligning it parallel to the polar axis renders it insulating. This behavior is a result of polarization discontinuity at the inclined walls, which induces electron charge accumulation and a sharp increase in the wall conductivity.²⁵ In PFM, this DW bending appears as a nanometer-range shift between the DW positions. Indeed, careful comparison of the PFM images of a poly-domain structure acquired after application of a positive and negative set bias reveals a DW displacement by about 10 nm even though the domain configuration remains largely intact (**Figs. 4c** and **4d**). These changes in DW conformation lead to the alternation between its high and low conductance states which could be directly detected by CAFM (**Figs. 4e** and **4f**, respectively). Although having a top electrode precludes detection of the individual DW conductance behavior, it can be reliably assumed that the same mechanism results in the conductance change of the poly-domain device. Thus, functional low-voltage memristive devices with the OFF/ON resistance ratio of up to 2 orders of magnitude can be realized based on modulation of DW conductance. Note that this approach provides more energy-

efficient, precise and reproducible tuning of device resistance. The resistance ratio could be further enhanced by using the domain structure with a higher density of the DWs. Furthermore, since there is no need for massive electrical cycling of polarization, the fatigue problem ceases to be an issue for this kind of devices.

The poly-domain structures generated in the Gr/LNO/Pt capacitors exhibit remarkably strong retention: we did not observe any noticeable decay over a period of 24 hours. This is in contrast to the significant domain relaxation over the same period of time in the LNO capacitors with oxide electrodes (see Figure S2). This difference could be related to more efficient screening of polarization in the capacitors with graphene. On the other hand, there is a partial decay in the induced conductance states (see Figure S3), which could be explained by the gradual change in the DW bending. It should be noted though that, in the Gr/LNO/Pt capacitors, this relaxation occurs at the time scale that is much longer than that observed for individual DWs²⁰ After conductance reduction by about 30% within 1 hour after application of a set pulse, there is a much slower relaxation to the 50% of the initial conductance value within a period of 14 hours. Although not completely non-volatile, this metastable tunable conductance does allow realization of a so-called plasticity effect used in the neuromorphic circuits.¹⁸ Along with the low operation voltage, this renders our Gr/LNO/Pt capacitors viable functional memristors.

In conclusion, we have investigated the resistive switching behavior related to the conducting DWs in the Gr/LNO/Pt capacitors. Two different mechanisms of resistance control have been employed to realize the DW-based memristive devices. The first one involves control of the conducting DW perimeter length via partial polarization reversal induced by super-coercive bias. The second one is based on modulation of the DW

conductance via application of non-switching sub-coercive bias to the device in the poly-domain state. This mechanism provides significant improvement in terms of energy cost, device resilience, lifetime, accuracy and reproducibility in controlling the resistance states in the Gr/LNO/Pt DW memristors. A big step forward here is that we have found a solid-state electrode, graphene, which does not get burned by the strong currents induced during the DW writing process in contrast to the delaminating metal electrodes. This finding along with the low-voltage operation paves the way for development of realistic functional memristive devices. Their high tunability demonstrated in this study enables their application in multi-level memories and neuromorphing applications.

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Author Contributions

P.C. and H.L. have equal contributions to the project. All the authors have given approval to the final version of this paper.

Notes

The authors declare no financial interests.

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Figure 1. Observation of conducting domain walls in LiNbO₃ thin films. (a) PFM phase image of the downward stripe domains created by scanning the film surface with the tip under +60 V bias. (b) CAFM map of the written domain pattern acquired using a dc 2 V bias. (c) PFM switching spectroscopy on bare surface. (d) TEM image of the sample cross-section showing electrically written domains.

Figure 2. Bias-dependent evolution of domain structure in the Gr/LNO/Pt capacitor.

(a) Topography of the graphene flake under study. (b-c) PFM phase images of the as-grown state (b), and after +33 V pulse (c), respectively, where polarization is transformed from the upward single domain state to a poly-domain state. (d-i) PFM phase images in the zoomed in region after application of poling pulses from +31 V to +37 V, and -10 V, respectively. All pulse durations were fixed at 5 s.

Figure 3. Tuning of the Gr/LNO/Pt capacitor resistance by a super-coercive bias. (a) The I-V characteristics in the Gr/LNO/Pt capacitor for the polydomain states created by poling pulses with an amplitude in the range from 31 V to 37 V, corresponding to the states shown in Figs. 2d-2h. (b) Device conductance as a function of total domain wall perimeter length. The inset shows the device conductance as a function of the poling pulse amplitude.

Figure 4. Tuning of the Gr/LNO/Pt capacitor resistance by a sub-coercive bias. (a) Conductance in the Gr/LNO/Pt capacitor as a function of set pulse amplitude for a poly-domain state created by a poling pulse of 33 V, 1 s. Set pulse duration was fixed at 1 s and conductance readout was at 2 V dc bias. (b) Device conductance as a function of set pulse duration for different set pulse amplitudes. A preset pulse of -2 V, 1 s (for positive set pulses) or 6 V, 1 s (for negative set pulses) was applied to reset the initial states. (c) PFM amplitude image of polydomain structure on the LNO bare surface. (d) Comparison of the domain wall positions using PFM imaging after application of negative and

positive dc set biases: red contour domain lines - after dc 10 V; black contour domain lines - after dc -1 V. While the domain structure is generally intact, there is a slight shift of the domain walls by about 10 nm after dc set biases of opposite polarities. (e,f) CAFM images of the domain walls shown in (c) illustrating a drastic change in domain wall conductance upon application of sub-coercive set bias.

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