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# A 5-GHz Class- $E_3F_2$ Power Amplifier with 51% PAE and 21-dBm Output Power on 65nm CMOS

Matthew Love<sup>1</sup>, Mury Thian<sup>1</sup>, and Andrei Grebennikov<sup>2</sup>

<sup>1</sup>Queen's University Belfast, Northern Ireland

<sup>2</sup>Sumitomo Electric Europe Ltd., United Kingdom

mlove05@qub.ac.uk; m.thian@qub.ac.uk; grandrei@ieee.org

**Abstract**— The design and simulation of a Class- $E_3F_2$  power amplifier using 65nm CMOS technology are detailed in this paper. The Class-EF amplifier combines aspects of the Class-E and -F load networks such as the harmonic terminations from the Class F and the use of a shunt capacitance at the drain in the Class E. A mixed-voltage cascode topology is used for the output stage to enable the use of fast low-voltage transistors with a higher supply voltage. To satisfy the Class-EF conditions the load network is designed to provide a short and open circuit to the second and third harmonic signals, respectively. The driver stage utilizes an Inverse Class-B topology to deliver a half-wave rectified sine to the output stage. The simulated amplifier achieved a power-added efficiency of 51% and a gain of 26 dB at an output power of 21 dBm. The second and third harmonic components were attenuated to -47.6 dBc and -79.3 dBc, respectively.

**Keywords**— Cascode, Class- $E_3F_2$ , CMOS, driver, finite choke, high efficiency, integrated circuits, Inverse Class-B, planar inductors, power amplifier, switched-mode.

## I. INTRODUCTION

Future wireless standards such as 5G are set to place greater strain on the power consumption of mobile devices due to the increased complexity required. This can be mitigated by improving the efficiency of the power amplifier (PA) as it consumes the largest power compared to other building blocks in a transceiver. Switched-mode PA topologies such as Class E [1]-[2] and F offer a theoretical maximum efficiency of 100% and thus have potential to deliver this increase in efficiency. The Class-EF PA described in [3] combines aspects of Class-E and -F PAs to harness benefits such as the integration of the device output capacitance into the load network as in the Class E and the drain voltage waveform shaping using harmonic tuning as in the Class F. As a result, the Class-EF topology offers a “soft switching” operation and a lower peak switch voltage than that of the Class E, which alleviates the issue of oxide breakdown in CMOS devices.

Silicon has made inroads into the RF space in recent years due to advanced fabrication techniques allowing switching speeds of over 200 GHz. It allows integration with the rest of the signal chain and removes the need for expensive technologies such as Gallium Arsenide (GaAs) and Indium Phosphide (InP).

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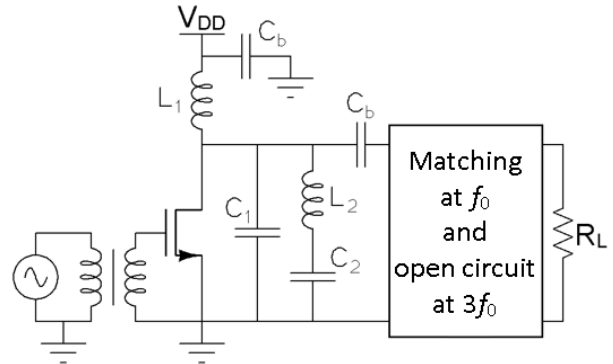


Fig. 1. The proposed Class- $E_3F_2$  power amplifier circuit topology.

However, the lossy nature of the silicon substrate results in major challenges in achieving a high power-added efficiency (PAE) for devices. The use of low frequencies prevents the use of transmission lines for matching. This instead is achieved through the use of lumped elements such as planar inductors which greatly suffer from low quality factors ( $Q$ ) and low inductance values. For the Class-EF PA this also means that only a few harmonics can be tuned in the load network.

In this paper the design of a 5-GHz Class- $E_3F_2$  amplifier on 65 nm CMOS using an Inverse Class-B driver will be detailed. An ideal switched-mode PA is typically driven with a square wave, which can be challenging to generate in reality. The Inverse Class B is employed as a driver as it provides a compromise in the form of a half-wave rectified sine output. Load-pull technique is used to find the optimal load impedance in order to maximize the PAE. The output matching network is designed to provide an open circuit to the third harmonic and simultaneously match the  $50 \Omega$  output resistance to the desired load. The Class- $E_3F_2$  PA was previously analyzed in [4] with a design being implemented using transmission lines. Here, a new Class- $E_3F_2$  topology suitable for lumped component realizations is proposed. The Class-EF naming convention is as follows: the subscript to the E describes the harmonics open-circuited at the load while the subscript to the F describes the harmonics shorted at the load. Therefore, in a Class- $E_3F_2$  amplifier, an open and short circuit are presented to the drain node of the transistor at  $3f_0$  and  $2f_0$ , respectively [4].

## II. INVERSE CLASS-B DRIVER AND CLASS-E<sub>3</sub>F<sub>2</sub> POWER AMPLIFIER TOPOLOGIES

The proposed Class-E<sub>3</sub>F<sub>2</sub> amplifier topology is shown in Fig 1. The  $L_2C_2$  resonator is tuned to  $2f_0$  to provide a short to ground. At  $f_0$ , the  $L_2C_2$  branch becomes capacitive and forms a parallel resonator with  $C_1$  and  $L_1$  tuned to  $f_0$ . At  $3f_0$ ,  $L_2C_2$  is inductive and forms a parallel  $3f_0$  resonator with  $C_1$  and  $L_1$ .  $C_b$  is a DC blocking capacitance. Equations (1)-(3) detail how to size  $C_1$ ,  $C_2$  and  $L_2$  when  $L_1$  is chosen by the designer. As  $L_1$  will be connected to the supply voltage, a small value should be chosen to maximize the  $Q$  and reduce the voltage drop. In order to fulfil the Class-EF conditions, the output matching network also needs to present an open circuit at  $3f_0$  to the drain of the transistor. This will cause the third-harmonic component to be reflected back to the drain, and the voltage waveform to steepen, reducing the current/voltage overlap hence improving the PAE.

$$C_1 = \frac{4}{9 \omega_0^2 L_1} \quad (1)$$

$$C_2 = \frac{5}{12 \omega_0^2 L_1} \quad (2)$$

$$L_2 = \frac{1}{4 \omega_0^2 C_2} \quad (3)$$

The Class E<sub>3</sub>F<sub>2</sub> combines elements from the load networks of the Class-E and -F topologies. At high frequencies, the output capacitance of a device results in a large transition time due to the charging-discharging process which in turn increases the losses in the Class-F topology. This power loss can be minimized by employing the zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions used in the Class E. An inductive load can introduce a dead time between device turn-OFF and turn-ON to allow the output capacitance to discharge before the next cycle. Fig. 2(a) shows the switch current and voltage waveforms of an ideal Class-E<sub>3</sub>F<sub>2</sub> amplifier. The quasi rectangular voltage waveform is similar to that of the Class F whereas the current waveform follows the Class E with the instantaneous drop to zero at the moment of device turn-OFF as the current is diverted through the shunt capacitance [5].

The Inverse Class-B circuit described in [6] generates a half-wave rectified sine wave, which provides an alternative for the square wave typically used to drive an ideal switched-mode PA. Like the Class B it employs a  $180^\circ$  conduction angle though the gate biasing voltage is set equal to the supply voltage so only the negative portion of the sine wave is conducted. It has a theoretical peak efficiency of 57.6% [6] which is lower than that of Class B, i.e., 78.5%. The current and voltage waveforms can be seen in Fig. 2(b).

Due to the low breakdown voltage in CMOS processes, the cascode topology is often used to reduce the peak switch voltage. A cascode amplifier also has a larger output impedance which makes it easier to match the output to  $50 \Omega$ . Importantly, it reduces the input sensitivity to the output impedance. However, it tends to have lower efficiency due to the reduced voltage swing caused by the use of the common-gate (CG) transistor.

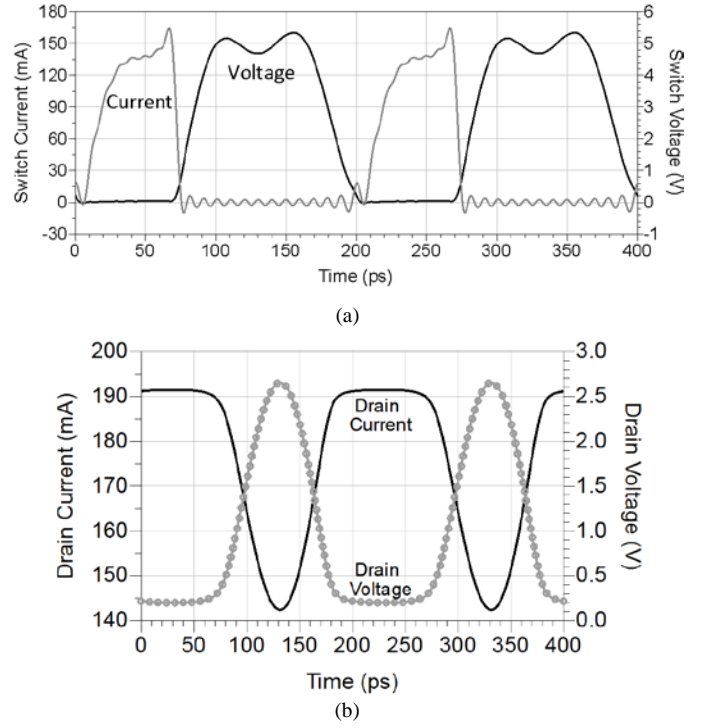


Fig. 2. Switch current and voltage waveforms: (a) idealized Class-E<sub>3</sub>F<sub>2</sub> power amplifier (5 GHz, 2.5 V, 20 dBm), and (b) Inverse Class-B driver.

The efficiency can be improved by using a mixed-voltage cascode topology, which is comprised of a fast low-voltage common-source (CS) transistor and a higher-voltage CG transistor. The CS transistor can switch faster to achieve higher efficiencies while the CG transistor enables the use of higher supply voltages. The detrimental effects of a large parasitic capacitance (including the device output capacitance),  $C_P$ , in a cascode amplifier can be reduced with the use of a series  $L_P C_B$  network connected between the transistors and ground.  $L_P$  is tuned to resonate with  $C_P$  and present an open circuit to the fundamental-frequency component, and  $C_B$  acts as a DC blocking capacitance.

## III. DESIGN METHODOLOGY: BRIDGING THE GAP BETWEEN THEORY AND IMPLEMENTATION

The driver is comprised of a 1 V 65 nm NMOS with a width of  $576 \mu\text{m}$  and a 0.5 nH dc-feed inductance. The gate and drain bias voltages are both set to 0.4 V to ensure Inverse Class-B operation and to limit the voltage to the output stage. The transistor is sized so that no inter-stage matching network is required, and this comes with a minor performance penalty. The DC component of the driver's output voltage waveform is suitable to bias the output stage. This removes the need for a DC blocking capacitance and an input biasing circuit for the output stage. The output stage is a mixed-voltage cascode with a  $1344 \mu\text{m}$  wide 1 V 65 nm NMOS in the CS configuration while the CG element used a 2.5 V 280 nm NMOS with a gate width of  $2016 \mu\text{m}$  and biased at 1.7 V. The series  $L_6C_8$  network in Fig. 3 is used to lessen the effect of the cascode output capacitance and improve the PAE.

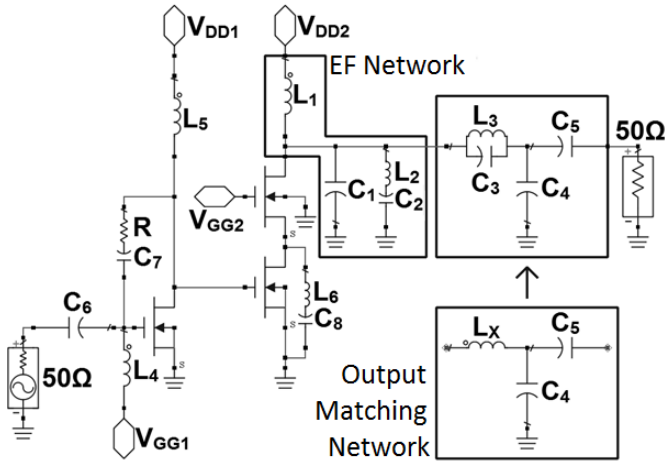


Fig. 3. Complete circuit schematic of the Inverse Class-B driver and Class-E<sub>3</sub>F<sub>2</sub> power amplifier. The EF network and output matching network are highlighted.

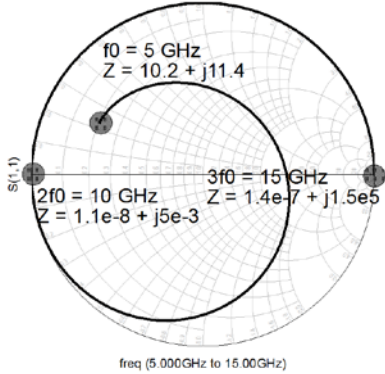


Fig. 4. Simulated load impedances of the proposed lumped-element Class-E<sub>3</sub>F<sub>2</sub> PA at fundamental, second and third harmonic frequencies.

The EF network shown in Fig. 3 is designed using (1)-(3).  $L_1$  is used in place of an ideal RF choke and is sized to 0.75 nH to maximize the PAE. The EF network is first tested using ideal components to ensure that the open and short circuit conditions are satisfied. The ideal components are then replaced with non-ideal models and are lightly tuned to reduce the effects of the models' imperfections.

A load-pull analysis is performed with the predetermined EF network attached to the drain of the transistor, Fig. 3. The impedance at the fundamental frequency  $10.2 + j11.4$  is chosen to maximize the PAE. A T-network  $L_x$ - $C_4$ - $C_5$  shown in Fig. 3 is used to match the  $50 \Omega$  load to the desired impedance. To satisfy the Class-EF requirement of an open circuit at  $3f_0$ , the parallel resonator  $L_3C_3$  is used in place of the inductor  $L_x$  and is designed using (4) and (5) to present the original value of  $L_x$  to the fundamental. Fig. 4 shows the PA load impedances at  $f_0$  to  $3f_0$ .

$$L_3 = \frac{8}{9} L_x \quad (4)$$

$$C_3 = \frac{1}{9 \omega_0^2 L_3} \quad (5)$$

TABLE I. CIRCUIT COMPONENT VALUES

$L_1 = 0.75$ nH ( $Q = 20.4$ )	$C_1 = 0.60$ pF
$L_2 = 0.45$ nH ( $Q = 19.8$ )	$C_2 = 0.56$ pF
$L_3 = 0.92$ nH ( $Q = 19.9$ )	$C_3 = 0.12$ pF
$L_4 = 0.63$ nH ( $Q = 21.8$ )	$C_4 = 0.94$ pF
$L_5 = 0.50$ nH ( $Q = 22.0$ )	$C_5 = 3.22$ pF
$L_6 = 1.07$ nH ( $Q = 18.4$ )	$C_6 = 0.75$ pF
$L_x = 1.03$ nH	$C_7 = 0.36$ pF
$R = 350 \Omega$	$C_8 = 4.08$ pF

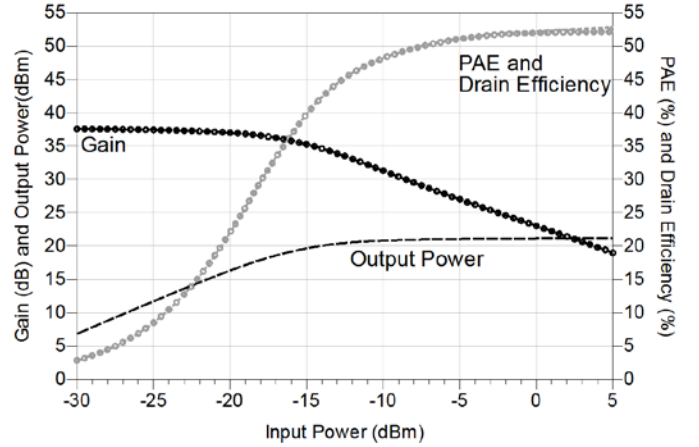


Fig. 5. Simulated gain, output power, PAE and drain efficiency versus input power.

TABLE II. SIMULATION RESULTS USING ACTUAL DEVICE MODELS

Parameter	Aimed	Achieved (Pin = -5 dBm)
Gain (dB)	> 20	26
P <sub>out</sub> (dBm)	> 20	21
Drain efficiency (%)	> 50	51.1
PAE (%)	> 50	51
2 <sup>nd</sup> harmonic level (dBc)	< -30	-47.6
3 <sup>rd</sup> harmonic level (dBc)	< -30	-79.3

The input matching is achieved using a simple yet effective high-pass-filter network with the inductor  $L_4$  and capacitor  $C_6$  doubling as the dc-feed and dc-blocking components, respectively. The series  $R$ - $C_7$  network is added to ensure unconditional stability from few MHz to 25 GHz. The final circuit component values are presented in Table I.

#### IV. SIMULATION RESULTS

Simulated gain, output power, PAE and drain efficiency are plotted versus input power in Fig. 5. The simulation results are presented against the targets in Table II. All targets are met with the harmonic suppression levels far exceeding the targets. The second harmonic was at -47.6 dBc with the third harmonic at -79.3 dBc. The output power spectrum up to  $10f_0$  illustrated in Fig. 6 shows high level of harmonic attenuation. This ensures that a clean sine wave will be delivered to the load. As can be seen from Fig. 7, the 3-dB bandwidth was 3.17 GHz ranging from 3.04 to 6.21 GHz.

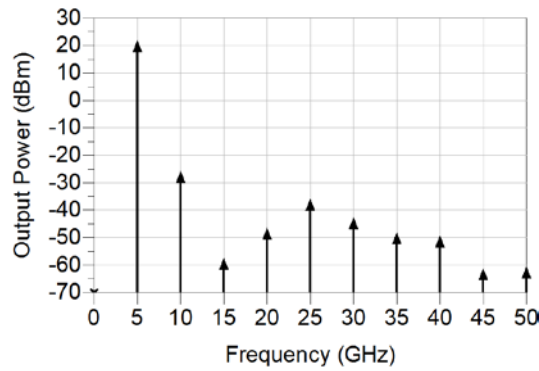


Fig. 6. Output power spectrum up to  $10f_0$ .

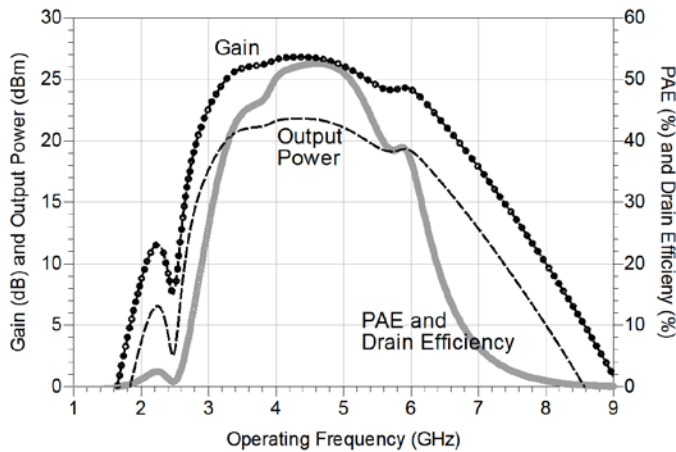


Fig. 7. Simulated gain, output power, PAE and drain efficiency versus operating frequency.

TABLE III. COMPARISONS WITH OTHER CMOS PAs

Parameter	This work*	[7]	[8]*	[9]	[10]	[11]*
Frequency (GHz)	5	5	5	2.5	2.4	2.2
Process (nm)	65	180	65	130	180	130
Supply (V)	2.5	2.3	1.36	2	2.4	3.3
Gain (dB)	26	21	9.3	31	31	N/A
Pout (dBm)	21	16.4	22.1	19	23	28.5
PAE (%)	51	35.4	40	32	42	47
Attenuation at $2f_0$ and $3f_0$ (dBc)	47.6/ 79.3	N/A	N/A	42/ 33	N/A	N/A

\*Simulation

## V. CONCLUSION

The design and simulation of a 5-GHz Class- $E_2F_3$  power amplifier using actual component models have been

successfully demonstrated. It utilized a two-stage approach with an Inverse Class-B amplifier providing a half-wave rectified sine driving input signal fed to a mixed-voltage cascode amplifier utilizing a Class-EF load network. The device achieved a PAE of 51% and an output power of 21 dBm at an input power level of -5 dBm. The use of the Class-EF load network resulted in excellent harmonic suppression levels with the second and third harmonic components attenuated to -47.6 and -79.3 dBc, respectively. Table III presents a comparison between this work and other similar designs.

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