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GENERALIZING ROOT VARIABLE CHOICE IN WAVE DIGITAL FILTERS WITH GROUPED NONLINEARITIES

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ABSTRACT

Previous grouped-nonlinearity formulations for Wave Digital Filter (WDF) modeling of nonlinear audio circuits assumed that nonlinear (NL) devices with memoryless voltage–current characteristics were modeled as voltage-controlled current sources (VCCSs). These formulations cannot accommodate nonlinear devices whose equations cannot be written as NL VCCSs, and they cannot accommodate circuits with cutsets composed entirely of current sources (including NL VCCSs). In this paper we generalize independent and dependent variable choice at the root of WDF trees to accommodate both these cases, and review two graph theorems for avoiding forbidden cutsets and loops in general.

1. INTRODUCTION

Along with State Space Modeling [14] and Port Hamiltonian Systems [5,8], the Wave Digital Filter (WDF) [9] formalism is a major approach to Virtual Analog modeling of audio circuits. In short, the Wave Digital Filter approach reframes an electrical circuit into a tree-like structure that separates electrical elements from their topological connections, represents each electrical element and topological connection mathematically with explicit input-output relationships in the (typically voltage or power) wave domain, discretizes reactive elements (most commonly using the trapezoidal rule), and resolves delay-free loops in the resulting structure by tuning the port resistance parameter of the wave variable definition at each port in the circuit. For circuits built entirely out of series and parallel connections, this approach is entirely modular. Good numerical behavior and incremental passivity can normally be inherited from passivity of the reference circuit and the use of wave variables [16]. The original WDF formalism could accommodate a single nonlinear electrical element at the root of the WDF tree [17], since typical audio circuits rather contain multiple nonlinear devices, handling multiple nonlinearities is currently a main subject of WDF research. Three recent approaches to handling multiple nonlinearities involve the resolution of fictitious delays in non-tree-like structures using techniques from multidimensional signal processing with convergence guaranteed in some cases by the contractive properties of passive circuit elements [18–21]. “Dynamic adaptation” of one-port nonlinearities which are not at the root [22], or global iterative solution over a WDF structure [23].

In this paper, we’ll deal with another recent thread in WDF research starting with [24] that is focused on solving the scattering matrices of complicated “R-type” adaptors [11] and the application of the topological insights of [25] (decomposition of a circuit graph into an SPQR tree) to generalized formulations for circuits involving multiple nonlinearities [12–13]. This approach groups all nonadaptable elements (most importantly nonlinearities) together at the root of a WDF tree 1 and interfaces that multipot root element to standard WDF subtrees using an $R$-type adaptor. Representing the mathematical relationships in this structure directly causes a number of delay-free loops in the signal flow graph, which may be resolved by a variety of methods.

Findings from this thread have enabled WDF simulation of circuits with complicated non-series/parallel topologies that may involve absorbed multiport linear elements [11] as well as multiple non-adaptable linear circuit elements [15] or nonlinear elements [12] grouped together at the root of a tree structure. These include audio circuits that were previously out of scope for WDF modeling: guitar tone stacks, active tone control circuits [11], the Hammond organ vibrato/chorus [15], circuits using operational amplifiers (modeled as ideal or using macromodels) [14] or operational transconductance amplifiers [27], Sallen–Key filters [28,29], guitar distortion stages [12], transistor [13] and triode [30] amplifiers, the Fender 5F6-A preamp stage [31], the Korg MS-50 Filter [32], relaxation oscillators [33], and the bass drum circuit from the Roland TR-808 Rhythm Composer [34].

However, two classes of circuits which may appear to be handled by those techniques on a topological level actually fail for reasons related to the choice of independent and dependent variables in the constituent equations of the circuits’ nonlinear devices. The first class of circuits involves nonlinear devices whose constituent equations are inherently written in a way that is incompatible with the previous WDF formulation [12]. The second class of circuits involves forbidden topological combinations of nonlinear devices with a certain mathematical description and ideal sources. Specifically these are circuits involving:

1. cutsets on the circuit graph composed entirely of nonlinearities with current as the dependent variable and ideal independent or controlled current sources; or
2. loops on the circuit graph composed entirely of nonlinearities with voltage as the dependent variable and ideal independent or controlled voltage sources.

These restrictions also apply in the context of State Space and Port Hamiltonian System modeling. In the State Space context, it is acknowledged that any node with only nonlinearities attached creates an inconsistent system if they are treated as controlled current sources, motivating the development of the Generalized State Space approach [4]. This is a special case of the restriction that a circuit may not contain any cutsets composed entirely of devices with current as the dependent variable. In the Port Hamiltonian System context, “implicit” formulations which in practice corre-

1 Similar to [26], although allowing root topologies other than parallel.
spond to series combinations of voltage-controlled (controlled current) components or parallel combinations of current-controlled (controlled voltage) components require extensions to the standard approach. These appear to be two special cases of the cutset and loop restrictions respectively. It is possible that the broader topological restrictions may not be widely recognized in audio circuit modeling since the most common problematic arrangement of diodes—series combinations of diodes and anti-parallel combinations of diodes in series—can be reasonably and intuitively modeled as a single one-port device in many circumstances. In this paper, we extend a WDF formalism involving grouped nonlinearities at the root of an SPQR tree to accommodate a wider variety of independent–dependent variable descriptions of nonlinear elements, enabling simulation of the two problematic classes of circuits mentioned above. For the first class of circuits, we exploit the proposed generalization to accommodate whatever pair of independent–dependent variables is required for each nonlinearity. For the second class of circuits, we explain the meaning of the forbidden topological connections and variable choices in terms of graph and network theory, give principles for choosing proper independent–dependent variable pairs, and show how to implement these principles using the proposed generalization. In this way, the class of problematic circuits which have been accommodated in the State Space and Port Hamiltonian context may be accommodated in the Wave Digital Filter context as well.

The rest of the paper is structured as follows. §2 outlines the proposed generalization to the WDF approach. §3 explains the first problematic class of circuits and how they can be accommodated using the proposed generalization. §4 explains the second problematic class of circuits and how they can be accommodated using the proposed generalization. To support a general search for problematic cutsets and loops, §5 reviews two graph theorems.

2. WDFs with Grouped Nonlinearities

In this section we review the method of grouped nonlinearities in WDFs, simultaneously extending it to handle nonlinearities and nonadaptable linear circuit elements expressed with a wide variety of independent and dependent variables.

2.1. Overview

The method of grouped nonlinearities in WDFs is outlined diagrammatically in Fig. 1. In this formulation there are five conceptual relationships to consider:

- All nonlinearities of the circuit grouped together into a nonlinear multiport element at the root of a tree structure (labeled “nonlinearities”). The behavior of the group of nonlinearities is expressed mathematically by \( y_c = f(x_c) \), where \( x_c \) is a vector of independent network port variables and \( y_c \) is a vector of dependent network port variables.
- A change of variables \( x_c \) and \( y_c \) to the vectors of incident and reflected voltage waves \( a_c \) and \( b_c \) (labeled “change of variables”), the subscript \( c \) denoting “converter.” This change of variables is expressed mathematically by the matrix \( C \) with partitions \( C_{11}, C_{12}, C_{21}, \) and \( C_{22} \).
- A compatibility relationship between \( a_c \) and \( b_c \) and “internal” port wave variables \( a_i \) and \( b_i \), simply enforcing port

\[
\begin{align*}
\text{Nonlinearities:} & \quad y_c = f(x_c) \\
\text{change of variables:} & \quad \begin{cases} x_c = C_{11}y_e + C_{12}a_e \\ b_c = C_{21}y_e + C_{22}a_e \end{cases} \\
\text{compatibility:} & \quad \begin{cases} a_c = b_c \\ a_i = b_i \end{cases} \\
\text{scattering:} & \quad \begin{cases} b_i = S_{11}a_i + S_{12}a_e \\ b_c = S_{21}a_i + S_{22}a_e \end{cases}
\end{align*}
\]

Some of the delay-free loops can be resolved using matrix algebra, yielding a consolidated version of (1–7) as follows:

\[
\begin{align*}
y_c &= f(x_c) \\
x_c &= E a_e + F y_e \\
b_c &= M a_e + N y_e
\end{align*}
\]
2.2. Populating S

To use the method just outlined, matrices S and C must be populated. S can be found using the techniques of [11], which applies Modified Nodal Analysis [39] to the R-type topology where instantaneous Thévenin equivalents represent the incident wave at each port, combining with the WDF wave definition to solve for S. If the R-type adaptor contains no absorbed non-reciprocal elements, the method of [40] may be used to solve for S.

2.3. New Considerations for C

In previous work, the nonadaptable root elements were usually modeled in the Kirchhoff domain by \( \dot{i} = f(v) \). This aligns with standard models for common electrical elements like diodes (Shockley model), BJT transistors (Ebers–Moll model), and triodes. So, the derivation of the C matrix assumed these Kirchhoff variables were to be converted to the wave variables \( a_n \) and \( b_n \).

In this work, we generalize that approach so that each entry in the vector of dependent (\( x_c \)) and independent (\( y_c \)) root variables may be a voltage, current, or wave variable. These may be “mixed and matched” in two senses. First, it is not required that each nonlinear element have the same independent or dependent variables. Second, it is possible to have, e.g., a Kirchhoff variable as an independent variable and a wave variable as a dependent variable (provided this still represents a single-valued function). It should be obvious that the independent and dependent variables at any port may not be linear combinations of one another.

In general, the relationship between the incident wave \( a_n \), and reflected wave \( b_n \) at a port \( n \) and two other variables which may

\[
E = C_{12}(I + S_{11}HC_{22})S_{12}, \quad F = C_{12}S_{11}HC_{21} + C_{11} \\
M = S_{21}HC_{22}S_{12} + S_{22}, \quad N = S_{21}HC_{21}
\]

where \( I \) is the identity matrix and \( H = (I - C_{22}S_{11})^{-1} \). This system of equations is shown as a vector signal flow graph in Fig. [15] notice that one delay-free loop through \( F \) and \( f(\cdot) \) remains. This delay-free loop can be resolved, e.g., by Newton–Raphson iteration [13], table lookup / the K method [12][38], custom nonlinear solvers [33], or a final matrix inversion in the case that all nonadaptable elements are linear [15].

2.4. New Considerations for f(\( \cdot \))

The E, M, and N matrix multiplies in Fig. [15] can be computed with no special considerations. However, the F matrix multiply and evaluation of the \( f(\cdot) \) vector nonlinear function evaluation form a delay-free loop, or implicit relationship. These can be combined into a zero-finding function

\[
x_c = E_a + Ff(x_c) \rightarrow h(x_c) = E_a + Ff(x_c) - x_c.
\]
Raphson iteration \([13]\) by first providing an initial guess \(x\) iterating according to

\[
\frac{dx}{dt} = \frac{\partial f}{\partial x}(x) \quad \text{or}\quad x_{n+1} = x_n - J(x_n)^{-1} f(x_n)
\]

where \(J(x_n)\) is the Jacobian matrix at \(x_n\). An alternative is given in \([13]\).

Typically we have \(f_2(\overline{i}_\text{out}, \overline{v}_\text{in}) = 0\), but \(f_1(\overline{i}_\text{out}, \overline{v}_\text{in})\) can take a number of forms, e.g.

\[
\text{clipper: } v_\text{out} = V_{\text{max}} \text{tanh} (A \overline{v}_\text{in}) \quad (21)
\]

\[
\text{comparator: } v_\text{out} = V_{\text{max}} \text{sgn} (\overline{v}_\text{in}) \quad (22)
\]

where \(A\) is the op amp’s gain in the clipper model (100,000 is typical) and \(V_{\text{max}}\) is the op amp saturation voltage in each model.

An example taken from \([33]\) of an audio circuit using an op amp configured as a comparator is a relaxation oscillator, shown in Fig. \(2a\). This circuit is rearranged as shown in Fig. \(2b\) yielding the WDF structure in Fig. \(2c\). The two ports of the nonlinearity are labeled “in” and “out.” The input variables \(x_c\) and output variables \(y_c\) are defined as in \([33]\). To accommodate this set of independent and dependent variables which are necessary for the op amp models just discussed we derive

\[
\frac{v_\text{out}}{v_\text{in}} = \frac{f_2(\overline{i}_\text{out}, \overline{v}_\text{in})}{f_1(\overline{i}_\text{out}, \overline{v}_\text{in})} = \frac{f(\overline{i}_\text{out}, \overline{v}_\text{in})}{f(\overline{i}_\text{out}, \overline{v}_\text{in})}.
\]

In the new generalized framework, elements of the vectors \(v\) and \(i\) are defined as in (20).

Typically we have \(f_2(\overline{i}_\text{out}, \overline{v}_\text{in}) = 0\), but \(f_1(\overline{i}_\text{out}, \overline{v}_\text{in})\) can take a number of forms, e.g.

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\frac{v_\text{out}}{v_\text{in}} = \frac{f_2(\overline{i}_\text{out}, \overline{v}_\text{in})}{f_1(\overline{i}_\text{out}, \overline{v}_\text{in})} = \frac{f(\overline{i}_\text{out}, \overline{v}_\text{in})}{f(\overline{i}_\text{out}, \overline{v}_\text{in})}.
\]
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4. SECOND CLASS OF PROBLEMATIC CIRCUITS

A second class of circuits that require the generalization presented in this paper are circuits that include cutsets composed entirely of nonlinearities (and current sources). In circuit theory, it is forbidden to have any cutset in a circuit graph composed entirely of current sources [41]. The presence of a cutset of current sources in a circuit creates the potential for a violation of Kirchhoff’s current law: the sum of currents leaving a node must equal the sum of currents entering that node. A dual restriction is that no loop in a circuit graph may be composed entirely of voltage sources [41]. The presence of a loop of all voltage sources creates the potential for a violation of Kirchhoff’s voltage law: the sum of voltages around any loop in the circuit must equal zero. This is a circuit theoretic argument but it is also expressed in the mathematics of the root topology. In the case of violating either the loop or the cutset criteria, it appears that in the WDF context the consequence is that the matrix \((I - C_{22}S_{11})\) which needs to be inverted is made singular. Examples will be given in the next section.

4 Anti-aliasing and multi-rate methods can be used to improve the simulation of the relaxation oscillator; these are described in Olsen et al. [33].

To fix this class of circuit, start with the standard choice of independent and dependent network variables for each nonlinearity. Identify each loop and cutset in the circuit by hand or using the graph theorems discussed in §5. If any problematic cutsets or loops exist, choose new dependent variables for some of the nonlinearities that make up that cutset or loop to avoid the issue.

4.1. Examples of Second Class

To discuss these issues, we consider three circuits: the “series diode clipper” shown in Fig. 4a, the “parallel diode clipper” shown in Fig. 4d and the “series–parallel diode clipper” shown in Fig. 4b.

Consider the series diode clipper and its WDF structure derivation shown in Fig. 4. Notice that inside the root topology \(S_1\) in Fig. 4a we have a node with only diodes connected to it. If the diodes were written in the form \(i = f(v)\), a current-source-only cutset is created. A remedy for this circuit would be to write either or both of the diodes in the form \(v = f(i)\), or more broadly in any form that does not have current as the dependent variable. In Tab. 2, the determinant of matrix \((I - C_{22}S_{11})\) is shown for the 49 different possible choices of \(x_1\) and \(y_1\) at port 1 (diode \(D_1\)) and port 2 (diode \(D_2\)). Notice that for the combinations that are forbidden according to circuit theory (both diodes with current as the dependent variable), the matrix which needs to be inverted becomes singular (its determinant is 0)—hence the circuit cannot be simulated using those variables.

It is not always a valid solution to choose voltage as the dependent variable. Consider the parallel diode clipper and its WDF structure derivation shown in Fig. 4. Notice that inside the root topology \(R_1\) in Fig. 4b there is a loop composed only of diodes. If the diodes were both written in the form \(v = f(i)\), a voltage-source-only loop is created, \((I - C_{22}S_{11})\) becomes singular, and

![Figure 4: Parallel clipper schematic and Derivation of Wave Digital Filter structure.](image-url)
the circuit cannot be simulated. For this circuit, it suffices that one or both diodes is written in the form \( i = f(v) \), or more broadly in any form that does not have voltage as the dependent variable. In Tab. 3, the determinant of matrix \((I - C_{22}S_{11})\) is shown for the 49 different possible choices of \(x_v\) and \(y_v\) at port 1 (diode \(D_1\)) and port 2 (diode \(D_2\)). Notice that for the combinations that are forbidden according to circuit theory (both diodes with voltage as the dependent variable), the matrix which needs to be inverted becomes singular (its determinant is 0)—hence the circuit cannot be simulated using those variables.

Sometimes it is necessary to choose different variables for each nonlinearity. For example, consider the series–parallel diode clipper shown in Fig. 5. Writing all three diodes in the form \( i = f(v) \) creates a current-source-only cutset but writing all three diodes in the form \( v = f(i) \) creates a voltage-source-only loop: both forbidden cases causing a singular matrix. Here the solution is that at least one diode is written with current as the dependent variable to avoid the loop, and that at least one of \(D_3\), \(D_5\) is written with voltage as the dependent variable to avoid the cutset.

5. ENUMERATING LOOPS AND CUTSETS ON GRAPHS

In the previous section we discussed circuits whose cutsets and loops were easily identifiable at a glance. Unfortunately in general circuits may be very complex and involve too many loops and cutsets to enumerate at a glance. To handle problematic circuits in general it is necessary to examine all loops and cutsets in the circuit graph and choose the dependent variables of the nonlinearities to avoid current-source-only cutsets and voltage-source-only loops. Here we review dual graph theorems for enumerating loops and cutsets in a graph (an alternative to identifying them by visual inspection as in the previous section) and demonstrate their application to two circuits discussed in §4.3.

5.1. Find All Loops in a Circuit

Here we review a theorem for enumerating the set of all loops in an electrical circuit and give example applications of the theorem for the parallel diode clipper.

The theorem is stated as follows [42, p. 50]:

1. Let the circuit be represented by a nonoriented, connected graph \(G\) with \(v\) vertices and \(e\) edges, where each vertex represents a node in the circuit and each edge represents a one-port electrical element in the circuit.

2. Choose a tree \(T\) on \(G\). Form a set of fundamental loops with respect to \(T\) by reinstanting each edge of the cotree \(T'\) one at a time to create fundamental loops involving each one edge and a tree path formed by some or all of the branches of \(T\). The fundamental loops are represented mathematically by a matrix \(B_T\) where each of the \(e \equiv v + 1\) fundamental loops is a row, and the \(v\) edges of \(G\) are the columns.

3. Form an intermediate matrix \(B_1\) by adding to \(B_T\) all the possible ring sums among the rows of \(B_T\). The ring sum of two sets \(S_1\) and \(S_2\) is the set \(S_1 \oplus S_2\) that has edges in \(S_1\) or \(S_2\) but not both [42, p. 14].

4. Eliminate redundant rows in \(B_1\), i.e. rows that appear more than once, to form \(B_n\), the loop matrix encoding all valid loops on \(G\). Redundant rows represent edge-disjoint unions of loops [42, p. 44].

Now, an example on the parallel diode clipper will illustrate the application of this theorem.

5.1.1. Parallel Diode Clipper Loops

Consider the parallel diode clipper whose schematic is shown in Fig. 6a. Using the mapping between electrical component and graph edges shown in Fig. 6b, a graph \(G\) of the parallel clipper is formed in Fig. 6c. \(G\) has 3 nodes \(\{v_a, v_b, v_c\}\) and 5 edges \(\{e_1, e_2, e_3, e_4, e_5\}\), i.e. \(v = 3\) and \(e = 5\).

To enumerate all loops on \(G\) we choose a tree \(T = \{e_2, e_3\}\) and corresponding co-tree \(T' = \{e_1, e_4, e_5\}\). Combining each edge \(e \in T'\) with other edges chosen from \(T'\) yields \(e - v + 1 = 3\) fundamental loops \(\{e_{c_1}, e_{c_4}, e_{c_5}\}\) encoded in a matrix \(B_T\)

\[
\begin{bmatrix}
0 & 1 & 1 & 1 & 1 & 0 \\
1 & 0 & 1 & 1 & 0 & 1 \\
1 & 0 & 0 & 1 & 1 & 0 \\
1 & 0 & 0 & 1 & 1 & 0 \\
1 & 0 & 0 & 1 & 1 & 0 \\
\end{bmatrix}
\]

We take all possible ring sums among the rows of \(B_T\) to find the intermediate matrix

\[
\begin{bmatrix}
0 & 1 & 1 & 0 & 0 & 0 \\
1 & 0 & 1 & 0 & 1 & 0 \\
1 & 0 & 0 & 1 & 0 & 0 \\
1 & 0 & 0 & 0 & 1 & 0 \\
1 & 0 & 0 & 0 & 0 & 1 \\
\end{bmatrix}
\]

The last ring sum represents an invalid loop, so it is discarded in forming \(B_n\). The final loop matrix \(B_n\) and graphical representation of the six loops \(\{c_1, c_2, c_3, c_4, c_5, c_6\}\) is given by

---

**Figure 5:** Series–parallel clipper schematic.

**Figure 6:** Parallel clipper (a) Schematic, (b) Mapping from circuit elements to graph edges, and (c) Graph.
To enumerate all cutsets on $G$ we choose a tree $T = \{e_2, e_3, e_4\}$ and corresponding cotree $T' = \{e_1, e_5\}$. Removing each edge $k \in T$ with other edges chosen from $T'$ yields $v - 1 = 3$ fundamental cutsets $\{k_{e_2}, k_{e_3}, k_{e_4}\}$ encoded in a matrix $Q_I$:

$$Q_I = \begin{bmatrix} k_{e_2} & k_{e_3} & k_{e_4} \\
11000 & 10101 & k_1 \\
00110 & 10110 & k_2 \\
01100 & 11010 & k_3 \\
\end{bmatrix}$$

We take all possible ring sums among the rows of $Q_I$ to find the intermediate matrix $Q_1$:

$$Q_1 = \begin{bmatrix} e_{1 e_2 e_3 e_4 e_5} \\
e_{1} & e_{2} & e_{3} & e_{4} & e_{5} \\
11000 & 10101 & 00110 & 10101 & 01100 \\
\end{bmatrix}$$

There are no redundancies in $Q_1$, so the final cutset matrix $Q_a$ and seven cutsets $\{k_1, k_2, k_3, k_4, k_5, k_6, k_7\}$ are given by:

$$Q_a = \begin{bmatrix} e_{1 e_2 e_3 e_4 e_5} \\
e_{1} & e_{2} & e_{3} & e_{4} & e_{5} \\
11000 & 10101 & 00110 & 10110 & 01100 \\
\end{bmatrix}$$

The third cutset $k_3 = \{e_4, e_5\}$ would be composed entirely of current sources if diodes $D_1, D_2$ (edges $e_4, e_5$) are modeled in the form $v = f(i)$, as we saw earlier.}

5.2. Find All Cutsets in a Circuit

Here we review a theorem for enumerating the set of all cutsets in an electrical circuit and give an example application of the theorem to a circuit discussed in §4, the series diode clipper.

The theorem is stated as follows [12, p. 58]:

1. Let the circuit be represented by a nonoriented, connected graph $G$ with $v$ vertices and $e$ edges.
2. Choose a tree $T$ on $G$. Form a set of fundamental cutsets with respect to $T$ by removing each edge of the cotree $T'$ one at a time to create fundamental cutsets each involving one tree edge and some or all of the edges of $T'$. The fundamental cutsets are represented mathematically by a matrix $Q_I$, where each of the $v - 1$ fundamental cutsets is a row, and the $e$ edges of $G$ are the columns.
3. Form an intermediate matrix $Q_1$ by adding to $Q_I$ all of the possible ring sums among the rows of $Q_I$.
4. Eliminate redundant rows in $Q_1$ to form $Q_a$, the cutset matrix encoding all valid cutsets on $G$.

Now, an example on the series diode clipper will illustrate the application of this theorem.

5.2.1. Series Diode Clipper Cutsets

Consider the series diode clipper whose schematic is shown in Fig. 7(a). Using the mapping between electrical component and graph edges shown in Fig. 7(b), a graph $G$ of the parallel clipper is formed in Fig. 7(c). $G$ has 4 nodes $\{v_n, v_i, v_c, v_d\}$ and 5 edges $\{e_1, e_2, e_3, e_4, e_5\}$, i.e., $v = 4$ and $e = 5$.
other benefits of flexibility in dependent variable choice for nonlinearity, the insights of this paper could be used in the other WDF formulations [18][23] which currently use wave variables only but also currently should not produce problematic cutsets or loops.

7. REFERENCES