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Broadband Parallel-Circuit Class-E Amplifier with Second Harmonic Control Circuit

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Abstract—This paper presents the analysis and coherent design method of a high-efficiency broadband parallel-circuit Class-E power amplifier with second harmonic control circuit. The PA’s broadband characteristic is achieved through analysis of the load network using double reactance compensation technique. Using a high power LDMOS transistor and operated from a 35 V supply voltage, the practical PA exhibits 41.5-44.1 dBm output power and 79-82.2% drain efficiency over 115-155 MHz frequency range. The measurement results show good agreements with the simulation results and theory.

Index Terms—Amplifier, broadband, Class-E, harmonic trap, high efficiency, parallel-circuit, reactance compensation.

I. INTRODUCTION

Switched-mode and harmonically tuned power amplifiers (PAs) have been widely used due to their simple structure and high efficiency characteristics, [1]-[8]. The Class-E with shunt capacitance topology reported in [6] and analyzed in [7] employs an ideal RF choke to provide an infinite impedance at both fundamental and harmonic frequencies, which renders its implementation challenging. In contrast, the parallel circuit Class-E topology described in [8] uses a finite dc-feed inductance, thereby offering compact size, low cost, and improved efficiency due to lower equivalent series resistance (ESR). Furthermore, when compared to the Class-E with shunt capacitance, the parallel-circuit Class-E PA offers higher maximum operating frequency and higher load resistance leading to a lower loss due to reduced impedance transformation ratio.

Wideband power amplifiers are required for deployment in modern wireless communication systems to enable high data rate transmission. Many techniques have been proposed to increase the inherent bandwidth of the Class-E PA, [9]-[15]. A differential wideband load transformation network was introduced in [9]. Using a combination of a finite dc-feed inductance and low-pass filters result in wideband Class-E amplifiers [10]. The work in [11] proposed a broadband lumped-element impedance matching technique that leads to high output power and high efficiency. However, this technique requires an additional network to transform 50Ω to the Class-E’s optimum load resistance. Wide bandwidth can also be achieved using reactance compensation techniques [12]-[15].

The basic circuits of the classical Class-E with shunt capacitance and the parallel-circuit Class-E power amplifier are shown in Fig. 1(a) and Fig. 1(b), respectively. In the Class-E mode, the current and voltage waveforms of the active device are shaped such that their overlap in time domain is minimal, thus minimizing power dissipation within the active device and maximizing the DC-to-RF efficiency. This is achieved through applying zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions.

In this paper, a new variant of the parallel-circuit Class-E PA is proposed, Fig. 1(c). The load network of the proposed circuit is comprised of a parallel-tuned resonator L-C where L doubles as a finite dc-feed inductance, a series-tuned resonator L0-C0 where C0 doubles as a finite dc-blocking capacitance, a second-harmonic trap composed of a parallel resonator L2-C2 in series with an inductor L2, and a resistor R. Compared with the parallel-circuit Class E, our circuit incorporates a second harmonic trap that is realized using a mixed parallel-series resonant circuit, i.e. L1-C1-L2. This load network is analyzed in the frequency domain using double reactance compensation technique to maximize the bandwidth of the proposed PA. The second harmonic trap circuit presents a low impedance to the ground to the second harmonic component whereas the series resonator L0-C0 presents a high impedance to other higher harmonic components (3rd, 4th, etc.) and prevents them from appearing at the output, thereby reducing the total harmonic distortion (THD) of the PA.

II. CIRCUIT ANALYSIS

The circuit schematic of the proposed PA and its equivalent circuit at the fundamental frequency (f0) are shown in Figs. 1(c)-(d). Both the series resonator L0-C0 and parallel resonator L1-C1 with the Queen’s University of Belfast, ECIT Institute, United Kingdom (e-mail: m.thian@qub.ac.uk). And Mehrnosh Vafaee is with Lorestan University (e-mail: mhrnsh.vafaee@gmail.com @gmail.com).
are tuned at $f_0$, thus provide a short and open circuit, respectively. At $2f_0$, the resonator $L_1-C_1$ behaves like a capacitance, which is resonated with $L_2$ to provide a short circuit. The circuit is analyzed using the following assumptions:

- The switch is on for $0 < \omega t < \pi$ and off for $\pi < \omega t \leq 2\pi$ interval, implying a 50% duty ratio.
- The output current is sinusoidal with the initial phase shift $\phi$.
- To simplify the analysis with an aim to arrive at some meaningful design insights, the transistor is modelled as an ideal switch in parallel with a shunt capacitor $C$. Large transistors typically employed in low-frequency high-power applications such as ours have low (negligible) $R_{ON}$ and considerably high $C_{OFF}$ values. Therefore, in our analysis, only $C_{OFF}$ is taken into account i.e. modelled as a linear capacitance $C$. In [16], it was shown that it is sufficient to approximate the nonlinear output capacitance of the transistor with a linear capacitance.

In the analysis of the idealized parallel-circuit Class-E PA [8], two optimum conditions, i.e., ZVS given in (1) and ZVDS given in (2) are applied. When the transistor is turned on, current flows through the switch but with no voltage produced across it. When the transistor is turned off, no current flows through the switch, and the switch voltage is equal to the voltage across the charged shunt capacitor $C$. Since the switch voltage and current do not overlap, no power is dissipated within the switch, resulting in a theoretical 100% DC-to-RF efficiency. Two quadrature fundamental-frequency currents $i_r$ and $i_x$ in Fig. 1(d) can be determined using Fourier integrals, and represented as the phase angle of the load network seen from the device drain at $f_0$, (3).

$$v(\omega t)|_{\omega t} = 2\pi = 0 \quad (1)$$
$$\frac{dv}{d\omega t}|_{\omega t} = 2\pi = 0 \quad (2)$$
$$\tan \phi = \frac{R}{\omega L} - \omega RC \quad (3)$$

The impedances of the series resonator $L_0-C_0$ and the parallel resonator $L_1-C_1$, denoted here as $Z_0$ and $Z_1$ respectively, can be expressed as

$$Z_0 = j\omega L_0 + \frac{1}{j\omega C_0} = j\omega L_0 \quad (4)$$
$$Z_1 = \frac{1}{j(\omega C_1 - \frac{1}{\omega L_1})} = \frac{1}{j\omega L_1} \quad (5)$$

where

$$\omega' = \omega^2 - \omega_0^2 \quad (6)$$
$$\omega_0^2 = \frac{1}{L_0 C_0} - \frac{1}{L_1 C_1} \quad (7)$$

The admittance of the load network, $Y_{net}$, can be expressed as

$$Y_{net} = \frac{1}{j\omega L} + j\omega C + \frac{1}{Z_A} \quad (8)$$

where

$$Z_A = Z_0 + \frac{1}{R + \frac{1}{Z_2}} \quad (9)$$

$$Z_2 = j\omega L_2 + Z_1 = j\omega L_2 + \frac{1}{j\omega' C_1} \quad (10)$$

Substitutions of (4) and (10) into (9) result in

$$Z_A = j\omega L_0 + \frac{R(\omega L_2 C_2 - 1)}{(\omega L_2 C_2 - 1) - j\omega' R C_1} \quad (11)$$

where

$$p = (\omega')^2 L_0 C_1 + m \quad (13a)$$
$$q = \omega' L_0 m \quad (13b)$$
$$m = \omega' L_2 C_1 - 1 \quad (13c)$$

$$\text{Im}\left(\frac{1}{Z_A}\right) = -\frac{(\omega'^2 C_1 p + m q)}{R^2 p^2 + q^2} \quad (12)$$

For specified DC supply voltage $V_{DD}$ (in V), output power $P_{out}$ (in W), and operating frequency $f_{on}$ (in rad/s), the optimum values of the parallel inductance $L$, capacitance $C$, and load resistance $R$ can be determined using (20)-(22) as derived in [8]:

$$L = 0.732 \frac{R}{\omega_0} \quad (20)$$
$$C = 0.685 \frac{\omega_0 R}{\omega_0} \quad (21)$$
$$R = 1.365 \frac{(V_{DD} - V_{sat})^2}{P_{out}} \quad (22)$$

where $V_{sat}$ is the saturation voltage of the switching device. The phase angle of the load network given in (3) can be determined using (20)-(22), yielding $\phi = 34.24^\circ$. Substitutions of (7), (19) and (20)-(22) into (15)-(16) result in

$$\frac{0.685}{\omega_0 R} + \frac{0.732 R_0}{R^2} - \frac{2L_0 - 2C_1 R^2}{R^2} = 0 \quad (23)$$
$$\frac{1}{0.122 \omega_0 R} + 48L_0 \left(\frac{L_0^2}{R^2} + C_2^2 - \frac{3\omega_0 C_1}{R^2}\right) = \frac{34}{3\omega_0} \left(\frac{L_0}{R^2} - C_1\right) \quad (24)$$

![Fig. 2. (a) Simulation setup, (b) ideal switch voltage and current waveforms.](image)
The values of $L_0$ and $C_1$ are determined by solving (23)-(24) simultaneously. The values of $C_0$, $L_1$ and $L_2$ are then calculated using (7) and (19).

### III. DESIGN PROCEDURES AND SIMULATIONS

In order to validate the analysis in Section II, we simulated the PA circuit in Fig. 1(c) using an ideal switch model and ideal passive components. The simulation setup with normalized frequency, DC supply voltage and output power is shown in Fig. 2(a). The switch current and voltage waveforms are shown in Fig. 2(b), from which it can be observed that the ZVS and ZVDS conditions are satisfied, and there is no overlap between the switch voltage and current waveforms, leading to a high efficiency close to 100%. The effect of variation in the switch voltage and current waveforms, leading to a high efficiency is shown in Fig. 2(b). From which it can be observed that as the duty ratio is increased, the peak switch voltage increases and the peak switch current decreases.

![Fig. 2](image-url)

The complete circuit schematic of the PA including the input matching network and gate biasing circuit is depicted in Fig. 3(a). The transistor used in our design is a high-ruggedness n-channel enhancement-mode lateral MOSFET (LDMOS) MRFE6V6225N from NXP Semiconductors with a drain-source breakdown voltage of 142 V and peak envelope power of 25 W [17]. Using a 35 V DC supply voltage, the PA was designed to deliver 30 W into a 50 Ω load across a 115-155 MHz frequency range.

![Fig. 3](image-url)

The theoretical and optimized values of the PA’s load network parameters are shown in Table I (all inductors are in nH and capacitors are in pF). The difference between the theoretical and optimized values of the shunt capacitor $C$ is mainly due to the transistor’s output capacitance, i.e. $C_{DS} = C_{oss} - C_{rss}$ where $C_{oss}$ and $C_{rss}$ are the output and reverse transfer capacitance of power MOSFET MRFE6V6225NR, respectively. An L-type input matching network, comprised of a series inductor 120 nH and a shunt capacitor 20 pF, is employed to match the input impedance of the MOSFET to the 50 Ω source impedance. The ESR of the 120 nH inductor, i.e. 15 Ω, helps improve the stability of the PA, resulting in stability factor (K) larger than 1 and stability measure (B1) larger than 0. The stability factor of the PA is shown in Fig. 4(b). The real and imaginary parts of the load network’s admittance, i.e. Re($Y_{net}$) and Im($Y_{net}$), are plotted versus frequency in Fig. 4(c), showing the effectiveness of the proposed load network to provide a

![Fig. 4](image-url)

**Table I**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>$L_0$</th>
<th>$C_0$</th>
<th>$L_1$</th>
<th>$C_1$</th>
<th>$L_2$</th>
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<td>Theoretical</td>
<td>42.8</td>
<td>16.2</td>
<td>97</td>
<td>14.3</td>
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<tr>
<td>Optimized</td>
<td>47</td>
<td>10</td>
<td>100</td>
<td>14</td>
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The values of $S$ are determined by solving (23)-(24) simultaneously. The values of $C_0$, $L_1$ and $L_2$ are then calculated using (7) and (19).

Fig. 1(a) Complete circuit schematic of the proposed PA. (b) Stability factor. (c) Real and imaginary parts of the load network’s admittance.

![Fig. 1](image-url)
constant conductance and susceptance over a wide frequency range.

![Fig. 5. Simulated drain voltage and current waveforms for $f_0 = (a) 115 \text{ MHz},$ (b) $135 \text{ MHz},$ and (c) $155 \text{ MHz}$.](image)

Illustrated in Fig. 5 are the simulated drain voltage and current waveforms for $f_0 = 115 \text{ MHz},$ $135 \text{ MHz},$ and $155 \text{ MHz},$ from which it can be observed that they resemble the standard Class-E mode waveforms. In particular, the peak drain voltage of the $115 \text{ MHz}$ case, i.e. $123 \text{ V}$, is in a good agreement with that of the parallel-circuit Class-E where $V_{\text{max}} = 3.647V_{\text{DD}}$. When simulated using the actual transistor model, an overlap between the switch voltage and current waveforms is inevitable due to nonidealties, packaging parasitics, etc., leading to a degradation in efficiency. To minimize this effect, a circuit optimization was performed using the built-in optimizer in ADS with a chief goal to maximize the efficiency while keeping the output power close to the specified value of $25 \text{ W}$. Fig. 6(a) shows that the PA load network presents a relatively constant impedance of $50 \Omega$ and a phase angle of around $34^\circ$ over the frequency range of interest. The simulated 2nd and 3rd harmonic suppression levels are depicted in Fig. 6(b). The proposed amplifier exhibits excellent 2nd and 3rd harmonic suppression of better than $30 \text{ dBc}$ from $125$ to $160 \text{ MHz}$. The 3rd harmonic suppression is achieved since the series resonator $L_0-C_0$ provides a high impedance (around $220 \Omega$) at $3f_0$. The simulated drain efficiency (DE), power added efficiency (PAE), and output power are plotted versus frequency in Fig. 7(a). The proposed PA with second harmonic control circuit and double reactance compensation technique is capable of providing maximum DE of $85\%$, PAE of $83.6\%$, and an output power of $44.3 \text{ dBm}$ over the $115$-$155 \text{ MHz}$ frequency range. The power gain compresses at $15 \text{ dBm}$ input power and efficiency reaches its maximum value at $26 \text{ dBm}$ input power. Shown in Fig. 7(b) are the DE and power gain versus output power, wherein the maximum DE is obtained at $44.3 \text{ dBm}$ output power.

![Fig. 6. (a) The impedance and phase angle of the PA load network, (b) second and third harmonic suppression levels.](image)

![Fig. 7. Simulated (a) DE, PAE, and output power versus frequency, (b) DE and power gain versus output power at $135 \text{ MHz}$.](image)

**IV. Measurements Results**

In order to validate the concept and analytical derivation described in Section II as well as the simulation results in Section III, we built a PA prototype on a $0.508 \text{ mm}$ RO4003C substrate with a dielectric constant of 3.55. The photograph of the PA is shown in Fig. 8(a) with an overall board size of 68
mm × 37 mm. The PA uses an MRFE6VS25N transistor with $V_{dd} = 2$ V as a switching device and Wurth inductors. The amplifier was driven by R&S 4320-MHz SMHU signal generator. The output power was measured using an Agilent Technologies 8563E spectrum analyzer. A 20-dB attenuator was inserted between the PA and the spectrum analyzer. The gate and drain voltages were applied using a MP3005D 30-VDC power supply. The simulated and measured input gate and drain voltages were applied using a MP3005D 30-VDC power supply. The output power was measured using an Agilent 5471B spectrum analyzer. The PA uses an MRFE6VS25N transistor with $V_{dd} = 2$ V as a switching device and Wurth inductors. The constructed prototype delivered a maximum DE of 82.2 % and maximum output power of 25 W.

### Table II: Comparison with other works.

<table>
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<th>Ref</th>
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<th>FBW (%)</th>
<th>Pout (W)</th>
<th>$\eta$ (PAE) (%)</th>
<th>$2^{nd}$/3$^{rd}$ HS (dBc)</th>
<th>Technology</th>
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<td>70/-</td>
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<td>LDMOS</td>
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<tr>
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<td>70/-</td>
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<td>GaN</td>
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<td>-</td>
<td>69/-</td>
<td>-</td>
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<td>25</td>
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<td>-30/-30</td>
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### References