Chapter 1: High-efficiency power amplifier design


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7. High-efficiency power amplifier design

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High efficiency of the power amplifier can be obtained by using overdriven Class-B, Class-F, or Class-E operation modes and their subclasses, depending on the technical requirements. In all cases, an efficiency improvement in practical implementation is achieved by providing the nonlinear operation conditions when an active device can simultaneously operate in pinch-off, active, and saturation regions, resulting in the nonsinusoidal collector current and voltage waveforms, symmetrical for Class-F and asymmetrical for Class-E operation modes. In Class-F power amplifiers analyzed in frequency domain, the fundamental-frequency and harmonic load impedances are optimized by short-circuit termination and open-circuit peaking to control the voltage and current waveforms at the device output to obtain maximum efficiency. In Class-E power amplifiers analyzed in time domain, an efficiency improvement is achieved by realizing the on/off active device switching operation (saturation and pinch-off modes) with special current and voltage waveforms so that high voltage and high current do not concur at the same time.

7.1. Class-F circuit design

The possibility to maximize efficiency in a vacuum-tube amplifier was firstly demonstrated in the late 1910s by a suitable choice of grid voltage with the corresponding anode arrangement to produce an anode current or voltage waveform which is composed principally of the fundamental frequency and third harmonic and has a “Meander”-like form [1]. It was proposed to use the load network with a third- or higher-harmonic trap in series to the anode in practical implementation, as shown in Fig. 7.1(a) [2, 3]. However, effect of the inclusion of a third-harmonic resonator was described and analyzed in detail only 1.5 decades later [4, 5]. It was shown that the symmetrical anode voltage waveform and level of its depression can be provided with opposite phase conditions at the waveform midpoints between the fundamental and third harmonic and optimum value of the ratio between their voltage amplitudes. In addition, it was noted that high operation efficiency can be achieved even when impedance of the third-harmonic resonator is equal or slightly greater than that of the fundamental tank. To maximize efficiency of the vacuum-tube amplifier with better approximating a square voltage anode waveform, it was also suggested to use an additional resonator tuned to the fifth harmonic, as shown in Fig. 7.1(b) [6].
Fig. 7.1. Biharmonic and polyharmonic Class-F power amplifiers.

Fig. 7.2. Fourier voltage and current waveforms with third and second harmonics, respectively.

Figure 7.2 shows that the shapes of the voltage and current waveforms can be significantly changed with increasing fundamental voltage amplitude by adding even one additional harmonic component being properly phased. For example, the combination of the fundamental-frequency and third-harmonic components being 180° out-of-phase at center points results in a flattened voltage waveform with depression in its center. It is clearly seen from Fig. 7.2(a) that the proper ratio between the amplitudes of the fundamental and third-harmonic components can provide the flattened voltage waveform with minimum depression and maximum difference
between its peak amplitude and amplitude of the fundamental component. Similarly, the combination of the fundamental-frequency and second-harmonic components, being in phase at the center points, flattens the current waveform corresponding to the maximum values of the voltage waveform and sharpens the current waveform corresponding to the minimum values of the voltage waveform, as shown in Fig. 7.2(b). The optimum ratio between the amplitudes of the current fundamental-frequency and second-harmonic components can maximize a peak value of the current waveform, with its minimized value determined by the device saturation resistance in a practical circuit. Thus, power loss due to the active device can be minimized because the results of the integration over period when the minimum voltage corresponds to the maximum current will give a small value compared with the power delivered to the load.

### 7.1.1. **Idealized Class-F mode**

Generally, an infinite number of the odd-harmonic tank resonators can maintain a square collector voltage waveform, also providing a half-sinusoidal current waveform. Figure 7.3(a) shows such a Class-F power amplifier with a multiple-resonator output filter to control the harmonic content of its collector (anode or drain) voltage and current waveforms, thereby shaping them to reduce dissipation and to increase efficiency [7].

![Fig. 7.3. Basic circuits of Class-F power amplifier with parallel resonant circuits.](image)

To simplify an analysis of a Class-F power amplifier, whose simplified equivalent circuit is shown in Fig. 7.3(b), the following several assumptions are introduced:

- Transistor has zero saturation voltage, zero saturation resistance, and infinite off-resistance, and its switching action is instantaneous and lossless.
- RF choke allows only a dc current and has no resistance.
- Quality factors of all parallel resonant circuits have infinite impedance at the corresponding harmonic and zero impedance at other harmonics.
There are no losses in the circuit except only into the load $R_L$.

- Operation mode with a 50% duty ratio.

To determine the idealized collector voltage and current waveforms, let us consider the distribution of voltages and currents in the load network, assuming the sinusoidal fundamental current flowing into the load as $i_R(t) = I_R \sin(\omega t)$, where $I_R$ is its amplitude. The voltage $v(t)$ across the switch can be represented as a sum of the dc voltage $V_{cc}$, the fundamental voltage $v_R = i_R R_L$ across the load resistor, and the voltage $v_{odd}$ across the odd-harmonic resonators,

$$v(t) = V_{cc} + v_{odd}(2n + 1)\omega t + v_R(t). \quad (7.1)$$

Because the time moment $t$ was chosen arbitrarily, by introducing a phase shift of $\pi$, Eq. (7.1) can be rewritten for periodical sinusoidal functions as

$$v(t + \pi) = V_{cc} - v_{odd}(2n + 1)\omega t - v_R(t). \quad (7.2)$$

Then, the summation of Eq. (7.1) and Eq. (7.2) yields

$$v(t) = 2V_{cc} - v(t + \pi). \quad (7.3)$$

From Eq. (7.3), it follows that the maximum value of the collector voltage cannot exceed a value of $2V_{cc}$ and the time duration with a maximum voltage of $v = 2V_{cc}$ coincides with the time duration with a minimum voltage of $v = 0$. Because the collector voltage is zero when the switch is turned on, the only possible waveform for the collector voltage is a square wave, composing of only dc, fundamental-frequency, and odd-harmonic components.

During the interval $0 < \omega t \leq \pi$ when the switch is turned on, the current $i(t)$ flowing through the switch can be written as

$$i(t) = I_0 + i_{even}(2n \omega t) + i_R(\omega t) \quad (7.4)$$

whereas during the interval $\pi < \omega t \leq 2\pi$ when the switch is turned off, the current $i(t + \pi)$ is equal to zero, resulting in

$$0 = I_0 + i_{even}(2n \omega t) - i_R(\omega t). \quad (7.5)$$

Then, by substituting Eq. (7.5) into Eq. (7.4), we can rewrite Eq. (7.4) as

$$i(t) = 2i_R(\omega t) = 2I_R \sin(\omega t) \quad (7.6)$$

from which it follows that the amplitude of the current flowing through the switch during the interval $0 < \omega t \leq \pi$ is two times greater than the amplitude of the fundamental current. Thus, in a general case of entire interval, Eq. (7.4) can be rewritten as

$$i(t) = I_R (\sin \omega t + | \sin \omega t |) \quad (7.7)$$

which means that the switch current represents half-sinusoidal pulses with the amplitude equal to double load current amplitude.
Consequently, for a purely sinusoidal current flowing into the load, which is shown in Fig. 7.4(a), the ideal collector voltage and current waveforms can be represented by the appropriate normalized waveforms shown in Fig. 7.4(b) and 7.4(c), respectively. Here, a sum of the fundamental and odd harmonics approximates a square voltage waveform and a sum of the fundamental and even harmonics approximates a half-sinusoidal collector current waveform. As a result, the shapes of the collector current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously. Such a condition, with symmetrical collector voltage and current waveforms, corresponds to an idealized Class-F operation mode with 100% collector efficiency.

A Fourier analysis of the current and voltage waveforms allows us to obtain the following equations for the dc current and the fundamental voltage and current components in the collector voltage and current waveforms:

The dc current $I_0$ can be calculated from Eq. (7.7) as

$$I_0 = \frac{1}{2\pi} \int_0^{\pi} 2I_R \sin \omega t \, dt = \frac{2I_R}{\pi}.$$  

The fundamental current component can be calculated from Eq. (7.7) as

$$I_1 = \frac{1}{\pi} \int_0^{\pi} 2I_R \sin^2 \omega t \, dt = I_R.$$  

![Fig. 7.4. Ideal waveforms of Class-F power amplifier.](image-url)
The fundamental voltage component can be calculated using Eq. (7.3) as

\[ V_1 = V_R = \frac{1}{\pi} \int_{\pi}^{2\pi} 2V_{cc} \sin(\omega t + \pi) d\omega t = \frac{4V_{cc}}{\pi} \]  

(7.10)

where \( V_R = I_R R_L \) is the fundamental voltage amplitude across the load resistor \( R_L \).

Then, the dc power and output power at the fundamental frequency are calculated by

\[ P_0 = V_{cc} I_0 = \frac{2V_{cc} I_R}{\pi} \]  

(7.11)

\[ P_1 = \frac{V_1 I_1}{2} = \frac{2V_{cc} I_R}{\pi} \]  

(7.12)

respectively, resulting in a theoretical collector efficiency with maximum value of

\[ \eta = \frac{P_1}{P_0} = 100\% \]  

(7.13)

In this case, the impedance conditions seen by the device collector for an idealized Class-F mode must be equal to

\[ Z_1 = R_i = \frac{8V_{cc}}{\pi^2 I_0} \]  

(7.14)

\[ Z_{2n} = 0 \quad \text{for even harmonics} \]  

(7.15)

\[ Z_{2n+1} = \infty \quad \text{for odd harmonics}. \]  

(7.16)

### 7.1.2. Class F with maximally flat waveforms

Although it is impossible to realize the ideal harmonic impedance conditions in practical implementation, the peaking of at least several current and voltage harmonic components can be provided to achieve a high operation efficiency of the power amplifier. The more the voltage waveform provided by higher-order harmonic components can be flattened, the less power dissipation due to flowing of the output current (when the output voltage is extremely small) occurs. To understand the basic design principles and to numerically calculate the power amplifier efficiency according to the contribution of an appropriate number of the harmonic components of voltage and current waveforms, it is convenient to use a design technique based on a Class-F approximation with maximally flat waveforms [8]. In this case, the load network is assumed ideal to deliver only the fundamental-frequency power to the load without loss. The active device represents an ideal multiharmonic current source with zero saturation voltage and output capacitance for providing instant switching between saturation and pinch-off operation regions. Flattening of the voltage and current waveforms to realize a Class-F operation can be accomplished by using odd-harmonic components to approximate a rectangular voltage waveform and even-harmonic components to approximate a half-sinusoidal current waveform given by
For the symmetrical flattened voltage waveforms shown in Fig. 7.5, the medium points where the voltage waveform reaches its maximum and minimum values are at $\omega t = \pi/2$ and $\omega t = 3\pi/2$, respectively. Maximum flatness at minimum voltage requires the even-order derivatives to be zero at $\omega t = 3\pi/2$. As the odd-order derivatives are equal to zero because $\cos(n\pi/2) = 0$ for odd $n$, it is necessary to define the even-order derivatives of the voltage waveform given by Eq. (7.17).

![Graph](image1)

![Graph](image2)

![Graph](image3)

**Fig. 7.5. Voltage waveforms for $n$th-harmonic peaking**

For the third-harmonic peaking when only the third-harmonic component together with the fundamental one is present, their optimum amplitudes are defined as

\begin{align*}
v(\omega t) &= V_{cc} + V_1 \sin \omega t + \sum_{n=3,5,7,...}^{\infty} V_n \sin n\omega t \quad \text{(7.17)} \\
\end{align*}

\begin{align*}
i(\omega t) &= I_0 - I_1 \sin \omega t - \sum_{n=2,4,6,...}^{\infty} I_n \cos n\omega t . \quad \text{(7.18)}
\end{align*}
\[ V_1 = \frac{9}{8} V_{cc} \quad V_3 = \frac{1}{8} V_{cc}. \]  
(7.19)

The voltage waveforms for the third-harmonic peaking \((n = 1, 3)\), fifth-harmonic peaking \((n = 1, 3, 5)\), and seventh-harmonic peaking \((n = 1, 3, 5, 7)\) are shown in Fig. 7.5.

For the symmetrical current waveforms shown in Fig. 7.6, the medium points where the current waveform reaches its minimum and maximum values are at \(\omega t = \frac{\pi}{2}\) and \(\omega t = \frac{3\pi}{2}\), respectively. As the odd-order derivatives are equal to zero because \(\cos(\frac{\pi}{2}) = 0\) and \(\sin(n\frac{\pi}{2}) = 0\) for even \(n\), it is sufficient to determine the even-order derivatives of the current waveform given by Eq. (7.18). Maximum flatness at minimum current requires the even-order derivatives to be zero at \(\omega t = \frac{\pi}{2}\).

For the second-harmonic peaking when only the second-harmonic component together with the fundamental one is present, their optimum amplitudes are defined by
\[ I_1 = \frac{4}{3} I_0 \quad I_2 = \frac{1}{3} I_0. \quad (7.20) \]

The current waveforms for the second-harmonic peaking \((n = 1, 2)\), fourth-harmonic peaking \((n = 1, 2, 4)\), and sixth-harmonic peaking \((n = 1, 2, 4, 6)\) are shown in Fig. 7.6.

The effectiveness of the operations modes with different voltage and current harmonic peaking can be compared by calculating the collector (drain) efficiency \(\eta\) of each operation mode according to

\[ \eta = \frac{P_1}{P_0} = \frac{1}{2} \frac{V_1}{V_{cc}} \frac{I_1}{I_0}. \quad (7.21) \]

The resultant efficiencies for various combinations of the voltage and current harmonic components are given in Table 7.1, which shows that the efficiency increases with an increase in the number of voltage and current harmonic components. To increase efficiency, it is more desirable to provide harmonic peaking in consecutive numerical order (both for voltage and current harmonic components) than to increase the number of the harmonic components into only voltage or current waveforms. Class-F operation becomes mostly effective in comparison with Class-B operation if at least third-voltage harmonic peaking and fourth-current harmonic peaking are realized. An inclusion of fifth-voltage harmonic component increases the efficiency to 83.3%. An additional inclusion of sixth-current harmonic component into the current waveform and a seventh-voltage harmonic component into the voltage waveform leads to efficiencies up to 94%.

<table>
<thead>
<tr>
<th>Current harmonic components</th>
<th>Voltage harmonic components</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1/2 = 0.500</td>
</tr>
<tr>
<td>1, 2</td>
<td>2/3 = 0.667</td>
</tr>
<tr>
<td>1, 2, 4</td>
<td>32/45 = 0.711</td>
</tr>
<tr>
<td>1, 2, 4, 6</td>
<td>128/175 = 0.731</td>
</tr>
<tr>
<td>1, 2, 4, ..., (\infty)</td>
<td>(\pi/4 = 0.785)</td>
</tr>
</tbody>
</table>

### 7.1.3. Class F with quarterwave transmission line

Ideally, a control of an infinite number of the harmonics maintaining a square voltage waveform and a half-sinusoidal current waveform at the device output can be provided by using a serious quarterwave transmission line and a parallel-tuned resonant circuit, as shown in Fig.
This type of a Class-F power amplifier was initially proposed to be used at higher frequencies, where implementation of the load networks with only lumped elements is difficult and the parasitic device output (lead or package) inductor is sufficiently small [9]. In this case, the quarterwave transmission line transforms the load impedance according to

\[ R = \frac{Z_0^2}{R_L} \]  

(7.22)

where \( Z_0 \) is the characteristic impedance of a transmission line. For even harmonics, the short circuit on the load side of the transmission line is repeated, thus producing a short circuit at the drain. However, the short circuit at the load produces an open circuit at the drain for odd harmonics with resistive load at the fundamental.

Fig. 7.7. Class-F power amplifier with series quarterwave transmission line.

Generally, at low drive level, the active device acts as a current source (voltage-controlled in the case of the MOSFETs or MESFETs and current-controlled in the case of bipolar transistors). As input drive increases, the active device enters saturation resulting in a harmonic-generation process. Because the quarterwave transmission line presents the high impedance conditions to all odd harmonics, all odd harmonics provide a proper contribution to the output voltage waveform. As a result, at high drive level, the output voltage waveform approximates a square wave, and the transistor is saturated for a full half-cycle. In this case, the transistor acts as a switch rather than a saturating current source.

An alternative configuration of the Class-F power amplifier with a shunt transmission line located in between the dc power supply and the device collector is shown in Fig. 7.8(a). In this case, there is no need to use an RF choke and a series blocking capacitor because a series fundamentally tuned resonant \( L_0C_0 \) circuit is used instead of a parallel fundamentally tuned resonant circuit. However, unlike the case with a series quarterwave transmission line, such a Class-F load-network configuration with a shunt quarterwave transmission line does not provide an impedance transformation. Therefore, the load resistance \( R \), which is equal to the equivalent active device output resistance at the fundamental frequency, must then be transformed to the
standard load resistance $R_t$. Let us now derive analytically fundamental properties of a quarterwave transmission line. The transmission line in time domain can be represented as an element with finite delay time depending on its electrical length. Consider a simplified load network of the Class-F power amplifier shown in Fig. 7.8(b), which consists of a parallel quarterwave transmission line grounded at the end through the dc power supply, a series fundamentally tuned $L_0C_0$ circuit, and a load resistance $R$. In an idealized case, the intrinsic device output capacitance is assumed to be negligible to affect the power amplifier performance. The loaded quality factor $Q_L$ of the series resonant $L_0C_0$ circuit is high enough to provide the sinusoidal output current $i_R$ flowing into the load $R$.

![Class-F power amplifier with shunt quarterwave transmission line.](image)

To define the collector voltage and current waveforms, consider the electrical behavior of a homogeneous lossless quarterwave transmission line connected to the dc voltage supply with RF grounding [10, 11]. In this case, the voltage $v(t, x)$ in any cross section of such a transmission line can be represented as a sum of the incident voltage $v_{inc}(\omega t - 2\pi x/\lambda)$ and the reflected voltage $v_{refl}(\omega t + 2\pi x/\lambda)$, generally with an arbitrary waveform. When $x = 0$, the voltage $v(t, x)$ is equal to the collector voltage,

$$v(\omega t) = v(t, 0) = v_{inc}(\omega t) + v_{refl}(\omega t). \quad (7.23)$$

At the same time, at another end of the transmission line when $x = \lambda/4$, the voltage is constant and equal to

$$V_{cc} = v(t, \pi/2) = v_{inc}(\omega t - \pi/2) + v_{refl}(\omega t + \pi/2). \quad (7.24)$$
Because the time moment $t$ was chosen arbitrarily, let us rewrite Eq. (7.24) using a phase shift of $\pi/2$ for each voltage by

$$v_{\text{inc}}(\omega t) = V_{cc} - v_{\text{refl}}(\omega t + \pi). \quad (7.25)$$

Substituting Eq. (7.25) into Eq. (7.23) yields

$$v(\omega t) = v_{\text{refl}}(\omega t) - v_{\text{refl}}(\omega t + \pi) + V_{cc}. \quad (7.26)$$

Consequently, for the phase shift of $\pi$, the collector voltage can be obtained by

$$v(\omega t + \pi) = v_{\text{refl}}(\omega t + \pi) - v_{\text{refl}}(\omega t + 2\pi) + V_{cc}. \quad (7.27)$$

For an idealized operation condition with a 50% duty ratio when during half a period the transistor is turned on and during another half a period the transistor is turned off with overall period of $2\pi$, the voltage $v_{\text{refl}}(\omega t)$ can be considered the periodical function with a period of $2\pi$,

$$v_{\text{refl}}(\omega t) = v_{\text{refl}}(\omega t + 2\pi). \quad (7.28)$$

As a result, the summation of Eqs. (7.26) and (7.27) results in the basic expression for collector voltage in the form

$$v(\omega t) = 2V_{cc} - v(\omega t + \pi). \quad (7.29)$$

From Eq. (7.29), which is similar to Eq. (7.3), it follows that the maximum value of the collector voltage cannot exceed a value of $2V_{cc}$ and the time duration with maximum voltage of $v = 2V_{cc}$ coincides with the time duration with minimum voltage of $v = 0$.

Similarly, the equation for the current $i_T$ flowing into the quarterwave transmission line can be obtained by

$$i_T(\omega t) = i_T(\omega t + \pi) \quad (7.30)$$

which means that the period of a signal flowing into the quarterwave transmission line is equal to $\pi$ because it contains only even harmonics, because a shorted quarterwave transmission line has an infinite impedance at odd harmonics at its input.

Let the transistor operate as an ideal switch when it is turned on during the interval $0 < \omega t \leq \pi$ where $v = 0$ and turned off during the interval $\pi < \omega t \leq 2\pi$ where $v = 2V_{cc}$, according to Eq. (7.29). During the interval $\pi < \omega t \leq 2\pi$ when the switch is turned off, the load is directly connected to the transmission line and $i_T = -i_R = -I_R \sin \omega t$. Consequently, during the interval $0 < \omega t \leq \pi$ when the switch is turned on, $i_T = I_R \sin \omega t$ according to Eq. (7.30). Hence, the current flowing into the quarterwave transmission line at any $\omega t$ can be represented by

$$i_T(\omega t) = I_R |\sin \omega t| \quad (7.31)$$

where $I_R$ is the amplitude of current flowing into the load.

Because the collector current is defined as $i = i_T + i_R$, then

$$i(\omega t) = I_R (\sin \omega t + |\sin \omega t|) \quad (7.32)$$
which means that the collector current represents half-sinusoidal pulses with the amplitude equal to double load current amplitude.

![Ideal current waveform in quarterwave transmission line.](image)

Consequently, for a purely sinusoidal current flowing into the load due to the infinite loaded quality factor of the series fundamentally tuned $L_0 C_0$ circuit shown in Fig. 7.4(a), the ideal collector voltage and current waveforms can be represented by the corresponding normalized square and half-sinusoidal waveforms shown in Figs. 7.4(b) and 7.4(c), respectively, where $I_0$ is the dc current. Here, a sum of odd harmonics approximates a square voltage waveform, and a sum of the fundamental and even harmonics approximates a half-sinusoidal collector current waveform. The waveform corresponding to the normalized current flowing into the quarterwave transmission line shown in Fig. 7.9 represents a sum of even harmonics. As a result, the shapes of the collector current and voltage waveforms provide a condition where the current and voltage do not overlap simultaneously.

7.1.4. Effect of saturation resistance

It is useful to analytically estimate the effect of a saturation (or on-resistance) $r_{sat}$ that is not equal to zero in a real transistor, and transistor therefore dissipates some amount of power due to the collector current flowing through this resistance when the transistor is turned on. The simplified equivalent circuit of a Class-F power amplifier with a quarterwave transmission line where the transistor is represented by a nonideal switch with the saturation resistance $r_{sat}$ and parasitic output capacitance $C_{out}$ is shown in Fig. 7.10. During the interval $0 < \omega t \leq \pi$ when the switch is turned on, the saturation voltage $v_{sat}$ due to the current $i(\omega t)$ flowing through the switch can be written as

$$v_{sat}(\omega t) = V_{sat} \sin \omega t = 2I_0 r_{sat} \sin \omega t$$  \hspace{1cm} (7.33)

where, by using Eq. (7.10), the saturation voltage amplitude $V_{sat}$ can be obtained by

$$V_{sat} = 2 V_0 \frac{r_{sat}}{R} = \frac{8 V_{dc} r_{sat}}{\pi R}.$$  \hspace{1cm} (7.34)
The corresponding collector current and voltage waveforms are shown in Fig. 7.11, where the half-sinusoidal current flowing through the saturation resistance $r_{sat}$ causes the deviation of the voltage waveform from the ideal square waveform. In this case, the bottom part of the voltage waveform becomes sinusoidal with the amplitude $V_{sat}$ during the interval $0 < \omega t \leq \pi$. From Eq. (7.29), it follows that the same sinusoidal behavior will correspond to the top part of the voltage waveform during the interval $\pi < \omega t \leq 2\pi$.

The power losses and collector efficiency due to presence of the saturation resistance $r_{sat}$ can be evaluated using Eqs. (7.6), (7.8), and (7.10) as

$$\frac{P_{sat}}{P_0} = \frac{1}{2\pi} \int_0^{2\pi} \frac{i^2(\omega t)r_{sat}}{I_0V_{cc}} \, d\omega t = \frac{r_{sat}}{2\pi I_0V_{cc}} \int_0^{2\pi} (2I_R)^2 \sin^2 \omega t \, d\omega t$$

$$= \frac{r_{sat}I_R}{V_{cc}} \frac{I_R}{I_0} = \frac{r_{sat}V_R}{R} \frac{I_R}{I_0} = \frac{2r_{sat}}{R}. \quad (7.35)$$

Hence, the collector efficiency can be calculated from

$$\eta = 1 - \frac{P_{sat}}{P_0} = 1 - \frac{2r_{sat}}{R}. \quad (7.36)$$
In practice, the idealized collector voltage and current waveforms can be realized at low frequencies when effect of the device output capacitance is negligible. At higher frequencies, effect of the output capacitance contributes to a nonzero switching time, resulting in time periods when the collector voltage and collector current exist at the same time when simultaneously \( v > 0 \) and \( i > 0 \). Consequently, such a load network with shunt capacitance cannot provide the switching-mode operation with an instantaneous transition from the device pinch-off to saturation mode and vice versa. Therefore, during a nonzero time interval, the device operates in the active region as a nonlinear current source.

### 7.1.5. Load networks with lumped and distributed parameters

Theoretical results show that the proper control of only second and third harmonics can significantly increase the collector efficiency of the power amplifier by flattening the output voltage waveform. Because practical realization of a multielement high-order \( LC \) resonant circuit can cause a serious implementation problem, especially at higher frequencies, it is sufficient to be confined to a three- or four-element resonant circuit composing the load network of the power amplifier. In addition, it is necessary to take into account that, in practice, the combined extrinsic and intrinsic transistor output capacitance has a substantial effect on the efficiency. The device output capacitance \( C_{\text{out}} \) can represent the collector capacitance \( C_c \) in the case of the bipolar transistor or the sum of the drain-source capacitance and gate-drain capacitance, \( C_{\text{ds}} + C_{\text{gd}} \), in the case of the FET device.

For a lumped-circuit power amplifier, a special three-element load network can be used to approximate the ideal Class-F mode by providing both high impedance at the fundamental and third harmonics and zero impedance at the second harmonic at the collector (or drain) by compensating for the influence of \( C_{\text{out}} \). Examples of such load networks with additional parallel and series resonant circuits located between the dc power supply and device output are shown in Fig. 7.12 [12, 13]. Here, the output circuit of the transistor is represented by a multiharmonic current source, and \( R_{\text{out}} \) is the equivalent output resistance at the fundamental frequency defined as a ratio of the fundamental voltage at the device output to the fundamental current flowing into the device.

The reactive part of the output admittance (or susceptance) \( B_{\text{net}} = \text{Im}(Y_{\text{net}}) \) of the load network with a parallel resonant tank shown in Fig. 7.12(b), including the device output capacitance \( C_{\text{out}} \), can be written as

\[
B_{\text{net}} = \omega C_{\text{out}} - \frac{1 - \omega^2 L_2 C_z}{\omega L_1 \left( 1 - \omega^2 L_2 C_z \right) + \omega L_2}.
\]  
(7.37)
By applying three-harmonic impedance conditions at the device collector (or drain), open-circuited for the fundamental and third harmonic when $B_{\text{net}}(\omega_0) = B_{\text{net}}(3\omega_0) = 0$ and short-circuited for the second harmonic when $B_{\text{net}}(2\omega_0) = \infty$, the parameters of this impedance-peeking load network can be derived as

$$L_1 = \frac{1}{6\omega_0^2 C_{\text{out}}} \quad L_2 = \frac{5}{3} L_1 \quad C_2 = \frac{12}{5} C_{\text{out}}$$

(7.38)

where the sum of the reactance of the parallel resonant tank, consisting of an inductor $L_2$ and a capacitor $C_2$, and an inductor $L_1$ create resonances at the fundamental and third-harmonics, whereas the series capacitive reactance of the tank circuit in series with the inductance $L_1$ creates a short-circuited series resonance condition at the second harmonic [12, 13].

Applying the same conditions for the load network with a series resonant circuit $L_2C_2$ shown in Fig. 7.12(c) results in the ratios between elements given by

$$L_1 = \frac{4}{9\omega_0^2 C_{\text{out}}} \quad L_2 = \frac{9}{15} L_1 \quad C_2 = \frac{15}{16} C_{\text{out}}$$

(7.39)

where an inductance $L_2$ and a capacitance $C_2$ create a short-circuited condition at the second harmonic, and all elements create the parallel-resonant tanks at the fundamental and third harmonics [14].

As a first approximation for comparison between different operation modes, the output device resistance $R_{\text{out}}$ at the fundamental frequency required to realize a Class-F operation mode
with third-harmonic peaking can be estimated as the equivalent resistance determined at
the fundamental frequency for an ideal Class-F operation and written as
\[ R_{\text{out}} = R_{\text{1(F)}} = \frac{V_1}{I_1}, \]
where \( V_1 \) and \( I_1 \) are the fundamental-frequency voltage and current amplitudes at the device
output, respectively. For the same supply voltage \( V_{cc} \) and output power \( P_1 \) at the fundamental,
assuming zero saturation voltage and using Eq. (7.14) yield
\[ R_{\text{1(F)}} = \frac{8}{\pi^2} \frac{V_{cc}}{I_0} = \frac{8}{\pi^2} \frac{V_{cc}^2}{P_1} = \left( \frac{4}{\pi} \right)^2 R_{\text{1(B)}}, \]
where \( R_{\text{1(B)}} = \frac{V_{cc}^2}{2P_1} \) is the output resistance at the fundamental in an ideal Class-B mode.

The ideal Class-F power amplifier with all even-harmonic short-circuit termination and
third-harmonic peaking achieves a maximum drain efficiency of 88.4% [8]. Such an operation
mode can be very conveniently realized by using the transmission lines in the load network.
The impedance-peaking load-network topology of such a transmission-line power amplifier is
shown in Fig. 7.13 [12, 13].

![Diagram](image)

Fig. 7.13. Transmission-line impedance-peaking circuit for Class F.

In this case, a quarterwave transmission line \( TL_1 \) located between the dc power supply
and the drain terminal provides short-circuit termination for even harmonics. The electrical
length \( \theta_3 \) of an open-circuit stub \( TL_3 \) is chosen to have a quarter wavelength at the third-har-
monic component to realize a short-circuited condition at the right end of the series transmission
line \( TL_2 \), whose electrical length \( \theta_2 \) should provide an inductive reactance to resonate with the
device output capacitance \( C_{\text{out}} \) at the third harmonic. As a result, the electrical lengths of the
transmission lines at the fundamental frequency can be obtained as
\[ \theta_1 = \frac{\pi}{2}, \quad \theta_2 = \frac{1}{3} \tan^{-1} \left( \frac{1}{\frac{1}{3Z_0} \omega_0 C_{\text{out}}} \right), \quad \theta_3 = \frac{\pi}{6}, \]
where \( Z_0 \) is the characteristic impedance of the series transmission line \( TL_2 \) and \( \omega_0 \) is the fund-
damental angular frequency.
7.1.6. **Design examples of Class-F power amplifiers**

The effectiveness of the Class-F load-network design technique is demonstrated based on the example of high-power 1.25-μm LDMOSFET amplifiers. The circuit schematic of the simulated 500-MHz single-stage lumped LDMOSFET power amplifier is shown in Fig. 7.14, where its load network corresponds to that shown in Fig. 7.12(b) and their parameters are calculated from Eq. (7.38). In this case, the total gate width of a high-voltage LDMOSFET device is 7×1.44 mm to achieve 8 W of output power. The drain efficiency and power gain of the power amplifier versus input power $P_{in}$ for the case of ideal inductors are given in Fig. 7.15(a). The drain efficiency over 75% is obtained due to a short-circuited condition at the second-harmonic and open-circuited condition at the third harmonic. Generally, it is important to provide high-impedance conditions at higher-order harmonics that can be readily done by using an output matching circuit with the series inductor as a first element. This shortens the switching time from pinch-off region to voltage-saturation region by better approximating the idealized drain voltage square waveform, as shown in Fig. 7.15(c).

As follows from Eq. (7.17) for a symmetrical voltage waveform, the initial phases for the fundamental-frequency and higher-order harmonics should be equal, which is easy to realize by short-circuited and open-circuited conditions. However, according to Eq. (7.18) for a half-sinusoidal current waveform, the phases for any higher-order harmonic component should differ from the phase for the fundamental frequency by 90°. This condition is easily realized in a Class-B load network, where the fundamental component of the drain voltage is in phase with the fundamental component of the drain current, but, for all higher-order current harmonics, the impedance of the resonant circuit will be capacitive because the drain current harmonics mostly flow through the shunt capacitor. Therefore, the accurate harmonic phasing is very important to improve effectiveness of a Class-F load network. The amplifier drain efficiency and power
gain will be significantly reduced if the values of the quality factor of the load-network inductors are sufficiently small. For example, the maximum value of the drain efficiency can reach only 71% when an inductor quality factor at the fundamental frequency is $Q_{\text{ind}} = 30$, as shown in Fig. 7.15(b).

![Graph showing drain efficiency, power gain, and voltage waveform.](image)

Fig. 7.15. Drain efficiency, power gain, and voltage waveform.

Therefore, it is preferred at high power level to use the load networks with microstrip lines. Figure 7.16 shows the equivalent circuit of a simulated 500-MHz single-stage microstrip LDMOSFET power amplifier using an active device with the same geometry. The input and output matching circuits represent a $T$-type matching circuit each, consisting of a series microstrip line, a parallel open-circuit stub, and a series capacitor. To provide even-harmonic short-circuit termination and third-harmonic peaking for a Class-F mode, an RF grounded quarterwave microstrip line and a combination of the series short-length microstrip line and open-circuit stub with electrical length of 30° at the fundamental frequency are used. Such an output circuit configuration approximates the square drain voltage waveform with a good accuracy, as shown in Fig. 7.17(a), and provides the drain efficiency over 75% with a maximum output power of 8 W, as shown in Fig. 7.17(b). The resulting smaller value of the drain efficiency
compared to the theoretically achievable one can be explained by the nonoptimized impedances at higher-order harmonics since, unlike a lumped inductor, the transmission line exhibits an equidistant impedance performance in the frequency domain with consecutive poles and zeros at the characteristic frequencies. This means that using a simple $T$-type transmission-line transformer does not provide high impedance conditions at all higher-order harmonics simultaneously.

Fig. 7.16. Simulated microstrip LDMOSFET Class-F power amplifier.

Fig. 7.17. Drain voltage waveform, efficiency, and power gain.

Figure 7.18 shows the circuit schematic of a 2-GHz microstrip GaN HEMT power amplifier operating in a Class-F mode [15]. The GaN HEMT device on a SiC substrate used in this power amplifier was provided by Cree having a 3.6-mm gate periphery and maximum operating frequency of about 40 GHz. Both input and output matching networks terminate the second, third, and fourth harmonics and some of the higher-order even harmonics using the quarterwave transmission lines. The device output impedance at the fundamental of 70 $\Omega$ was chosen for the
design as it was a good tradeoff of efficiency and output power. In this case, the load network provides the impedance matching at the fundamental and the corresponding Class-F harmonic control at the second, third, and fourth harmonics simultaneously. The fundamental matching was provided by choosing the optimum value of the transmission-line characteristic impedances $Z_2$ and $Z_3$. Tuning the output matching network which includes the device output capacitance resulted in a very high third-harmonic impedance of about 400 Ω, whereas the impedances at the second and fourth harmonics were of about 0.5 Ω and 0.7 Ω, respectively. Note that high impedance at the fundamental with corresponding high supply voltage was chosen to minimize the effect of the parasitic bondwire and package inductors to provide the near short-circuited Class-F conditions at the second and higher-order even harmonics, whose effect becomes significant at higher operating frequencies. An input matching network was designed to provide a second-harmonic short by using a quarterwave transmission line close to the gate and conjugate matching at the fundamental. Two shunt RC networks at the input were added to provide the stability of operation. As a result, the power amplifier achieved the maximum drain efficiency of 87% and power-added efficiency (PAE) of 83% at an output power of 17.8 W and at a drain supply voltage of 42.5 V, with a maximum power gain of 15.8 dB and its compressed value of 13.4 dB at peak PAE.

7.2. Inverse Class F

Effect of the inclusion of the parallel resonant circuit tuned to the second harmonic and located in series at the anode, as shown in Fig. 7.19(a), was first described and analyzed in the early 1940s [5, 16]. It was shown that the symmetrical anode current waveform and level of its depression can be provided with the opposite phase conditions between the fundamental-frequency and second-harmonic components and an optimum value of the ratio between their voltage amplitudes. It was noted that high operation efficiency can be achieved even when impedance of the tank circuit to second harmonic is equal or slightly greater than that of the tank circuit to fundamental frequency. In practical vacuum-tube amplifiers intended for operation at very high frequencies, the peak output power and anode efficiency can therefore be increased
by 1.15 to 1.2 times [17]. In addition, it was suggested to use an additional resonator, tuned to the fourth harmonic and connected in series with the second-harmonic resonator, as shown in Fig. 7.19(b), to maximize the anode efficiency of the vacuum-tube amplifier with approximate square voltage-driving waveform [18].

As a simple solution to realize 180° out-of-phase conditions between the voltage fundamental-frequency and second-harmonic components at the device output in vacuum-tube amplifiers, it was proposed to use a second-harmonic tank resonator connected in series to the device input [16]. Such an approach makes it possible to flatten the anode voltage waveform in active region avoiding the device saturation mode. In this case, the driver stage is loaded by the nonlinear diode-type input grid impedance of the final-stage tube providing a flattened grid voltage waveform, which includes the fundamental-frequency and second-harmonic components. The presence of the strong second-harmonic component results in a second-harmonic voltage drop across the resonator. The loaded quality factor of the second-harmonic resonator must be high enough to neglect the voltage drop at the fundamental frequency. As a result, the second-harmonic resonator has no effect on the voltage fundamental-frequency component. However, it provides a phase shift of 180° for the second-harmonic component, as increasing in a voltage drop across the resonator results in decreasing in the voltage drop across the grid-cathode terminals.

Figure 7.20 shows that the shapes of the voltage and current waveforms can be significantly transformed with increased voltage peak factor and current flattening by adding one additional harmonic component with a proper phase. For example, the combination of the fundamental-frequency and third harmonic components with 180° out-of-phase shift at the center of symmetry results in a flattened current waveform with depression in its center, as shown in Fig.
7.20(a), which can be minimized by using the proper ratio between the amplitudes of the fundamental and third harmonics. Similarly, the combination of the fundamental and second harmonics, which are in phase at the center of symmetry, sharpens the voltage waveform corresponding to minimum values of the voltage waveform, as shown in Fig. 7.20(b).

![Image of Fourier current and voltage waveforms with third and second harmonics.]

Fig. 7.20. Fourier current and voltage waveforms with third and second harmonics.

7.2.1. **Idealized inverse Class-F mode**

Generally, an infinite number of even-harmonic tank resonators can maintain a square current waveform with a half-sinusoidal voltage waveform at the collector. Figure 7.21(a) shows the basic schematic of an inverse Class-F power amplifier with a multiple-resonator output filter to control the harmonic content of its collector (anode or drain) voltage and current waveforms, thereby shaping them to reduce dissipation and to increase efficiency. The term “inverse” means that collector voltage and current waveforms are interchanged compared to a conventional case under the same idealized assumptions. Consequently, for a purely sinusoidal current flowing into the load, the ideal collector current waveform is composed by the fundamental component and odd harmonics approximating a square waveform. At the same time, the collector voltage waveform is composed by the fundamental component and even harmonics approximating a half-sinusoidal waveform. As a result, the shapes of the collector current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously, similarly to a conventional Class-F mode. Such a condition, with symmetrical collector
voltage and current waveforms, corresponds to an idealized inverse Class-F operation mode with 100% collector efficiency.

\[ i(\omega t) = 2I_0 - i(\omega t + \pi) \quad (7.42) \]

where \( I_0 \) is the dc current, and

\[ v(\omega t) = V_R (\sin \omega t + |\sin \omega t|) \quad (7.43) \]

where \( V_R \) is fundamental-frequency amplitude at the load. From Eq. (7.42), it follows that maximum value of the collector current cannot exceed that of \( 2I_0 \), and the time duration with maximum amplitude defined as \( i = 2I_0 \) coincides with that with minimum amplitude defined as \( i = 0 \). Because the collector current is zero when the switch is turned off, the only possible waveform for the collector current is a square wave composing of only dc, fundamental-frequency, and odd-harmonic components.

By using a Fourier analysis of the current and voltage waveforms, the following equations for the dc voltage, fundamental voltage and current components in the collector voltage and current waveforms can be obtained:

The fundamental current component can be calculated using Eq. (7.42) as

\[ I_1 = I_R = \frac{1}{\pi} \int_0^{\pi} 2I_0 \sin(\omega t + \pi) d\omega t = \frac{4I_0}{\pi}. \quad (7.44) \]

The dc voltage \( V_{cc} \) can be calculated from Eq. (7.43) as

\[ V_{cc} = \frac{1}{2\pi} \int_0^{\pi} 2V_R \sin \omega t d\omega t = \frac{2V_R}{\pi}. \quad (7.45) \]

The fundamental voltage component can be calculated from Eq. (7.43) as
Then, the relationship between the dc power $P_0$ and the output power at the fundamental frequency $P_1$ can be given as

$$P_1 = \frac{V_1 I_1}{2} = \frac{1}{2} \pi \frac{V_{cc}}{V_0} \frac{4I_0}{\pi} = P_0$$ (7.47)

resulting in a theoretical collector efficiency of 100%.

The impedance conditions seen by the device collector for an idealized inverse Class-F mode must be equal to

$$Z_1 = R_1 = \frac{\pi^2 V_{cc}}{8 I_0}$$ (7.48)

$$Z_{2n+1} = 0 \quad \text{for odd harmonics}$$ (7.49)

$$Z_{2n} = \infty \quad \text{for even harmonics.}$$ (7.50)

### 7.2.2. **Inverse Class F with quarterwave transmission line**

An idealized inverse Class-F operation mode can be represented by using a sequence of the series resonant circuits tuned to the fundamental and odd harmonics, as shown in Fig. 7.22(a). In this case, it is assumed that each resonant circuit has zero impedance at the corresponding fundamental frequency $f_0$ and odd-harmonic components $(2n + 1)f_0$ and infinite impedance at even harmonics $2nf_0$ realizing the idealized inverse Class-F square current and half-sinusoidal voltage waveforms at the device output terminal. As a result, the transistor which is driven to operate as a switch sees the load resistance $R_L$ at the fundamental frequency, whereas the odd harmonics are shorted by the series resonant circuits.

An infinite set of the series resonant circuits tuned to the odd harmonics can be effectively replaced by a quarterwave transmission line with the same operating capability. Such a circuit representation of an inverse Class-F power amplifier with a series quarterwave transmission line loaded by the series resonant circuit tuned to the fundamental frequency is shown in Fig. 7.22(b) [7, 19]. The series-tuned output circuit presents a load resistance at the frequency of operation to the transmission line. At the same time, the quarterwave transmission line transforms the load impedance according to

$$R = \frac{Z_0^2}{R_L}$$ (7.51)

where $Z_0$ is the characteristic impedance of a transmission line. For even harmonics, the open circuit on the load side of the transmission line is repeated, thus producing an open circuit at
the drain. However, the quarterwave transmission line converts the open circuit at the load to a short circuit at the drain for odd harmonics with resistive load at the fundamental frequency.

\[
V_{dd}, Z_0, \frac{\lambda}{4} \text{ (a)}
\]

\[
\text{v}_{in}, R_L, C_0, L_0, C_b, R_b. \text{ (b)}
\]

Fig. 7.22. Inverse Class-F power amplifier with series quarterwave transmission line.

Consequently, for a purely sinusoidal current flowing into the load due to infinite loaded quality factor of the series fundamentally tuned circuit, the ideal drain current and voltage waveforms can be represented by the corresponding normalized square and half-sinusoidal waveforms, respectively. Here, a sum of odd harmonics approximates a square current waveform, and a sum of the fundamental and even harmonics approximates a half-sinusoidal drain voltage waveform. As a result, the shapes of the drain current and voltage waveforms provide a condition when the current and voltage do not overlap simultaneously. The quarterwave transmission line causes the output voltage across the load resistor \( R_L \) to be phase-shifted by 90° relative to the fundamental-frequency components of the drain voltage and current.

7.2.3. Load networks with lumped and distributed parameters

Theoretical results show that the proper control of the second harmonic can significantly increase the collector efficiency of the power amplifier by flattening of the output current waveform and minimizing the product of integration of the voltage and current waveforms. Practical realization of a multi-element high-order \( LC \) resonant circuit can cause a serious implementation problem, especially at higher frequencies and in monolithic integrated circuits, when only three harmonic components can be effectively controlled. Therefore, it is sufficient to be confined to the three- or four-element resonant circuit composing the load network of the power amplifier. In this case, the operation with the second-harmonic open circuit and third-harmonic short circuit is a promising concept for low-voltage power amplifiers [20].
In addition, it is necessary to take into account that, in practice, both extrinsic and intrinsic transistor parasitic elements such as the output shunt capacitance or serious inductance have a substantial effect on the efficiency. The output capacitance $C_{\text{out}}$ can represent the collector capacitance $C_c$ in the case of the bipolar transistor or the sum of drain-source capacitance and gate-drain capacitance, $C_{\text{ds}} + C_{\text{gd}}$, in the case of the FET device. The output inductance $L_{\text{out}}$ is generally composed of the bondwire and lead inductances for a packaged transistor, whose effect becomes significant at higher frequencies.

![Diagram](image)

**Fig. 7.23. Second-harmonic impedance-peaking circuit.**

Figure 7.23 shows the equivalent circuit of the second-harmonic impedance-peaking load network, where the series circuit consisting of an inductor $L_1$ and a capacitor $C_1$ creates a resonance at the second harmonic. Because the device output inductance $L_{\text{out}}$ and capacitance $C_{\text{out}}$ are tuned to create an open-circuited condition at the second harmonic, the device collector sees resultant high impedance at the second harmonic. To achieve the second-harmonic high impedance, an external inductance may be added to interconnect the device output inductance $L_{\text{out}}$ directly at the output terminal (collector or drain) if its value is not sufficient. As a result, the values of the load-network parameters are defined as

$$L_{\text{out}} = \frac{1}{4\omega_0^2 C_{\text{out}}} \quad L_1 = \frac{1}{4\omega_0^2 C_1}.$$  \hspace{1cm} (7.52)

As a first approximation for comparison between different operation classes, the output device resistance $R_{\text{out}}$ at the fundamental frequency required to realize an inverse Class-F operation mode with second-harmonic peaking can be estimated as an equivalent resistance $R_{\text{out}} = R_{1}^{(\text{invF})}$ determined at the fundamental frequency for an ideal inverse Class-F mode. For the same supply voltage $V_{cc}$ and output power $P_1$ at the fundamental, assuming zero saturation voltage and using Eqs. (7.14) and (7.48) yield

$$R_{1}^{(\text{invF})} = \frac{\pi^2}{8} \frac{V_{cc}}{I_0} = \left(\frac{\pi^2}{8}\right)^2 R_{1}^{(F)} = \left(\frac{\pi}{2}\right)^2 R_{1}^{(B)}$$  \hspace{1cm} (7.53)

where $R_{1}^{(F)}$ is the output resistance at the fundamental frequency in a conventional Class-F mode and $R_{1}^{(B)}$ is the output resistance at the fundamental frequency in an ideal Class-B mode.
The ideal inverse Class-F power amplifier cannot provide all the voltage required by the third- and higher-order odd harmonic short-circuit termination using a single parallel transmission line, as can be easily realized by a quarterwave transmission line for even harmonics in the conventional Class-F power amplifier. In this case, with a sufficiently simple circuit schematic convenient for practical realization, applying the current second-harmonic peaking and voltage third-harmonic shorting can result in a maximum drain efficiency of more than 80% [21]. The output impedance-peaking load network of such a microstrip power amplifier is shown in Fig. 7.24, and its circuit structure is similar to that used to provide a conventional Class-F operation mode.

As it follows from Eq. (7.53), the equivalent output resistance for an ideal inverse Class-F mode is higher by more than 2.4 times compared to a conventional Class-B mode. Therefore, using an inverse Class-F mode simplifies the corresponding load-network design by minimizing the impedance transformation ratio. This is very important for high output power level with a sufficiently small load impedance. However, maximum amplitude of the output voltage waveform can exceed the supply voltage by about three times. In this case, it is required to use the device with high breakdown voltage or to reduce the supply voltage. The latter, however, is not desirable because it may result in lower power gain and efficiency.

For such an inverse Class-F microstrip power amplifier, it is necessary to provide the following electrical lengths for the transmission lines at the fundamental frequency:

\[
\theta_1 = \frac{\pi}{3}, \quad \theta_2 = \frac{1}{2} \tan^{-1}\left(\frac{2Z_0\omega_0 C_{\text{out}} + \frac{1}{\sqrt{3}}}{1}\right), \quad \theta_3 = \frac{\pi}{4} \tag{7.54}
\]

where \(Z_0\) is the characteristic impedance of the microstrip lines. The transmission line \(TL_1\) with electrical length \(\theta_1 = 60^\circ\) at the fundamental frequency provides a short-circuited condition for the third harmonic and introduces a capacitive reactance at the second harmonic. The open-circuit stub \(TL_3\) with electrical length \(\theta_3 = 45^\circ\) creates a short-circuited condition at the right
end of the transmission line $TL_2$ at the second harmonic. Thus, the transmission line $TL_2$ having an inductive reactance is tuned to the parallel resonance condition at the second harmonic with the device output capacitance $C_{out}$ and short-circuited transmission line $TL_1$.

### 7.2.4. Design example of inverse Class-F power amplifier

In a hybrid power amplifier where the packaged device is used, the presence of a transistor output series bondwire and lead inductance $L_{out}$ creates some problems in providing an acceptable second- or third-harmonic open- or short-circuit termination. In this case, it is convenient to use a series transmission line as a first element of the load network connected to the device output, as shown in Fig. 7.25(a), where the transmission line $TL_1$ is placed between the device drain and shunt short-circuited quarterwave transmission line $TL_3$. However, if the length of a combined series transmission line $TL_1 + TL_2$ becomes very long in a Class-F mode with a short circuit at the second harmonic and an open circuit at the third harmonic and additional fundamental-frequency matching circuit is required, then such a load network in an inverse Class-F mode is compact, convenient for harmonic tuning, and very practical.

![Fig. 7.25. Transmission-line inverse Class-F power amplifier and its equivalent circuit.](image)

Figure 7.25(b) shows the equivalent circuit of a transmission-line inverse Class-F load network, where the complex-conjugate load matching is provided at the fundamental frequency. Both high reactance at the second harmonic and low reactance at the third harmonic are created at the device output by using two series transmission lines $TL_1$ and $TL_2$, whose electrical lengths depend on the values of the device output shunt capacitance $C_{out}$ and series inductance $L_{out}$, quarterwave short-circuit stub $TL_3$, and open-circuit stub $TL_4$ with electrical length of $30^\circ$ [10, 22]. The output shunt capacitance $C_{out}$ can represent both intrinsic bias-dependent drain-source
capacitance $C_{ds}$ and extrinsic bias-independent drain pad-contact capacitance $C_{dp}$ of the nonlinear large-signal equivalent circuit for GaN HEMT device, whereas the series output inductance $L_{out}$ is modeled by a combined effect of the metallization, bond wire, and package inductances [23].

The harmonic conditions for an inverse Class-F load network seen by the device multiharmonic current source derived from Eqs. (7.48) through (7.50) for the first three harmonic components including fundamental are

$$\text{Re} Z_{\text{net}}(\omega_0) = R \quad (7.55)$$

$$\text{Im} Z_{\text{net}}(2\omega_0) = \infty \quad (7.56)$$

$$\text{Im} Z_{\text{net}}(3\omega_0) = 0 \quad (7.57)$$

where the load resistance (or equivalent output resistance) $R$ seen by the device output at the fundamental frequency is defined in an ideal inverse Class-F mode by Eq. (7.53).

Infinite reactance at second harmonic

Zero reactance at third harmonic

Fig. 7.26. Load networks seen by the device output at corresponding harmonics.

Figure 7.26(a) shows the transmission-line load network seen by the device multiharmonic current source at the fundamental frequency, where the combined series transmission line $TL_1 + TL_2$ (together with an open-circuit capacitive stub $TL_4$ with electrical length of $30^\circ$) provides an impedance matching between the optimum equivalent output device resistance $R$.
and the standard load resistance \( R_L \) by proper choice of the transmission-line characteristic impedances \( Z_1 \) and \( Z_2 \), where \( C_{out} \) and \( L_{out} \) are the elements of the matching circuit. For simplicity of calculation, the characteristic impedances of the transmission lines \( TL_1 \) and \( TL_2 \) are set to be equal to \( Z_1 \).

The load network seen by the device current source at the second harmonic (considering the short-circuit effect of the grounded quarterwave transmission line \( TL_3 \)) is shown in Fig. 7.26(b), where the transmission line \( TL_1 \) provides an open-circuited condition for the second harmonic at the device output by forming a second-harmonic tank together with the shunt capacitor \( C_{out} \) and series inductance \( L_{out} \). Similar load network at the third harmonic is shown in Fig. 7.26(c), where the open-circuit effect of the grounded quarterwave transmission line \( TL_3 \) and short-circuit effect of the open-circuit stub \( TL_4 \) at the third harmonic are used. In this case, the combined transmission line \( TL_1 + TL_2 \), which is short-circuited at its right-hand side and connected in series with an inductance \( L_{out} \) provides a short-circuited condition for the third harmonic at the device output. Depending on the actual physical length of the device package lead, the on-board adjustment of the transmission lines \( TL_1 \) and \( TL_2 \) can easily provide the required open-circuited and short-circuited conditions (as well as an impedance matching at the fundamental frequency) because of their series connection to the device output.

By using Eqs. (7.56) and (7.57), the electrical lengths of the transmission lines \( TL_1 \) and \( TL_2 \), assuming the same characteristic impedance \( Z_1 \) for both series transmission-line sections, can be defined from

\[
2\omega_0 C_{out} - \frac{1}{2\omega_0 L_{out} + Z_1 \tan 2\theta_i} = 0 
\]

\[
3\omega_0 L_{out} + Z_1 \tan 3(\theta_i + \theta_2) = 0 
\]

with the maximum total electrical length \( \theta_1 + \theta_2 = \pi/3 \) or \( 60^\circ \) at the fundamental frequency or \( 180^\circ \) at the third harmonic when \( L_{out} = 0 \).

As a result, the electrical lengths of the transmission lines \( TL_1 \) and \( TL_2 \) as analytical functions of the device output series inductance \( L_{out} \) and shunt capacitance \( C_{out} \) are obtained as

\[
\theta_1 = \frac{1}{2} \tan^{-1} \left( 1 - \frac{(2\omega_0)^2 L_{out} C_{out}}{2Z_1 \omega_0 C_{out}} \right) 
\]

\[
\theta_2 = \frac{\pi}{3} - \frac{1}{3} \tan^{-1} \left( \frac{3\omega_0 L_{out}}{Z_1} \right) - \theta_1 
\]

where the transmission-line characteristic impedance \( Z_1 \) can be set in advance. In order to omit an additional matching section at the fundamental frequency, the inverse Class-F load network can also be used to match the equivalent device fundamental-frequency impedance \( R \) with the
standard load impedance $R_L$ (usually equal to 50 $\Omega$). In this case, it is necessary to properly optimize both characteristic impedances $Z_1$ and $Z_2$.

![Image](image_url)

**Fig. 7.27.** Transmission-line 10-W inverse Class-F GaN HEMT power amplifier.

Figure 7.27(a) shows the test board of a transmission-line inverse Class-F power amplifier based on a 28-V 10-W Cree GaN HEMT power transistor CGH40010P and transmission-line load network with the second- and third-harmonic control, as shown in Fig. 7.25(a). The input matching circuit provides the fundamental-frequency complex-conjugate matching with the standard 50-$\Omega$ source. The parameters of the series transmission line in the load network were optimized for implementation convenience. In this case, the device input and output package leads as external elements were properly modeled to take into account effect of their inductances, and their models were then added to the simulation setup. The simulation results of a transmission-line inverse Class-F GaN HEMT power amplifier shown in Fig. 7.40(b) are based on a nonlinear device model supplied by Cree and technical parameters for a 30-mil RO4350 substrate. The maximum output power of 41.3 dBm, power gain of 13.3 dB (linear gain of about 18 dB), drain efficiency of 80.3%, and $PAE$ of 76.5% are achieved at an operating frequency of 2.14 GHz with a supply voltage of 28 V and a quiescent current of 40 mA. The experimental results of the test board shown in Fig. 7.27(a) were very close to the simulated results obtaining a maximum output power of 41.0 dBm, a drain efficiency of 76.0%, a $PAE$ of 72.2%, and a power gain of 13.0 dB at an operating frequency of 2.14 GHz (gate bias voltage $V_g = -2.8$ V and drain supply voltage $V_{dd} = 28$ V), achieved without any tuning of the input matching circuit and load network [10].
7.3. **Class E with shunt capacitance**

In late 1940s and early 1950s, during experimental tuning of the vacuum-tube amplifiers operating in a saturation mode, it was noticed and then concluded that, when the second and higher-order harmonics are properly phased, efficiency significantly increases when the load contains reactive components for harmonics, which form the proper shapes of anode voltage and current [24]. In this case, detuning of the resonant circuit is provided in the direction of higher frequencies when the operating frequency is lower than the resonance frequency of the resonant circuit. As a result, anode efficiencies of about 92 to 93% were achieved for the phase angles of the output load network within 30° to 40°, resulting in the proper inductive impedance at the fundamental frequency and capacitive reactances at the harmonic components seen by the anode of the active device [25]. A few years later, it was discovered that very high efficiencies could be obtained with a series resonant LC circuit connected to a transistor [26]. The exact theoretical analysis of the single-ended switching-mode power amplifier with a shunt capacitance and a series LC circuit was then given by Kozyrev [27].

7.3.1. **Optimum load-network parameters**

The single-ended switching-mode power amplifier with a shunt capacitance was introduced as a Class-E power amplifier by Sokals in 1975, and it has found widespread application because of its design simplicity and high operation efficiency [28, 29]. This type of high-efficiency power amplifiers was then widely used in different frequency ranges and with different output power levels ranging from several kilowatts at low RF frequencies up to about 1 W at microwaves [30]. The characteristics of a Class-E power amplifier can be determined by defining its steady-state collector voltage and current waveforms. The basic circuit of a Class-E power amplifier with shunt capacitance is shown in Fig. 7.28(a), where the load network consists of a capacitor $C$ shunting the transistor, a series inductor $L$, a series fundamentally tuned $L_0C_0$ circuit, and a load resistor $R$. In a common case, a shunt capacitance $C$ can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The collector of the transistor is connected to the supply voltage by an RF choke with high reactance at the fundamental frequency. The transistor is considered an ideal switch that is driven in such a way as to provide the instant device switching between its on-state and off-state operation conditions. As a result, the collector current and voltage waveforms are determined by the switch when it is turned on and by the transient response of the load network when the switch is turned off.
To simplify the analysis of a Class-E power amplifier, whose simplified equivalent circuit is shown in Fig. 7.28(b), the following assumptions are introduced:

- the transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching action is instantaneous and lossless
- the total shunt capacitance is independent of the collector and is assumed linear
- the RF choke allows only a constant dc current and has no resistance
- the loaded quality factor $Q_L = \omega L_0 / R = 1 / \omega C_0 R$ of the series resonant $L_0 C_0$ circuit tuned to the fundamental frequency is high enough for the output current to be sinusoidal at the switching frequency
- there are no losses in the circuit except only in the load $R$
- for simplicity, a 50% duty ratio is used.

For a lossless operation mode, it is necessary to provide the following optimum conditions for voltage across the switch (just prior to the start of switch on) at $\omega t = 2\pi$, when transistor is saturated:

$$ v(\omega t)_{\omega t=2\pi} = 0 $$

(7.62)

$$ \frac{dv(\omega t)}{d\omega t} \bigg|_{\omega t=2\pi} = 0 $$

(7.63)

where $v(\omega t)$ is the voltage across the switch.

The detailed theoretical analysis of a Class E power amplifier with shunt capacitance for any duty ratio is given in [31], where the load current is assumed to be sinusoidal,

$$ i_b(\omega t) = I_R \sin(\omega t + \varphi) $$

(7.64)

where $\varphi$ is the initial phase shift.
When the switch is turned on for $0 \leq \omega t < \pi$, the current through the capacitance

$$i_c(\omega t) = \omega C \frac{dv(\omega t)}{d\omega t} = 0$$  \hspace{1cm} (7.65)

and, consequently,

$$i(\omega t) = I_0 + I_R \sin(\omega t + \varphi)$$  \hspace{1cm} (7.66)

under the initial on-state condition $i(0) = 0$. Hence, the dc current can be defined as

$$I_0 = -I_R \sin \varphi$$  \hspace{1cm} (7.67)

and the current through the switch can be rewritten by

$$i(\omega t) = I_R \left[ \sin(\omega t + \varphi) - \sin \varphi \right].$$  \hspace{1cm} (7.68)

When the switch is turned off for $\pi \leq \omega t < 2\pi$, the current through the switch $i(\omega t) = 0$, and the current flowing through the capacitor $C$ can be written as

$$i_c(\omega t) = I_0 + I_R \sin(\omega t + \varphi)$$  \hspace{1cm} (7.69)

producing the voltage across the switch by the charging of this capacitor according to

$$v(\omega t) = \frac{1}{\omega C} \int_0^{\omega t} i_c(\omega t) d\omega t$$

$$= -\frac{I_R}{\omega C} \left[ \cos(\omega t + \varphi) + \cos \varphi + (\omega t - \pi) \sin \varphi \right].$$  \hspace{1cm} (7.70)

Applying the first optimum condition given by Eq. (7.62) enables the phase angle $\varphi$ to be determined as

$$\varphi = \tan^{-1}\left(-\frac{2}{\pi}\right) = -32.482^\circ.$$  \hspace{1cm} (7.71)

As a result, the normalized steady-state collector voltage waveform for $\pi \leq \omega t < 2\pi$ and current waveform for $0 \leq \omega t < \pi$ are

$$\frac{v(\omega t)}{V_{cc}} = \pi \left( \frac{\omega t - 3\pi}{2} - \frac{\pi}{2} \cos \omega t - \sin \omega t \right)$$  \hspace{1cm} (7.72)

$$\frac{i(\omega t)}{I_0} = \frac{\pi}{2} \sin \omega t - \cos \omega t + 1.$$  \hspace{1cm} (7.73)

Figure 7.29 shows the normalized (a) load current, (b) collector voltage waveform, and (c) collector current waveforms for an idealized optimum (or nominal) Class-E mode with shunt capacitance. From collector voltage and current waveforms, it follows that, when the transistor is turned on, there is no voltage across the switch, and the current $i(\omega t)$, consisting of the load sinusoidal current and dc current, flows through the device. However, when the transistor is turned off, this current is flowing through the shunt capacitor $C$. The jump in the collector current waveform at the instant of switching off is necessary to obtain nonzero output power at the
fundamental frequency delivered to the load, which can be defined as an integration of the
product of the collector voltage and current derivatives over the entire period [32].

Fig. 7.29. Normalized (a) load current and collector (b) voltage and (c) current wave-
forms for idealized optimum Class E with shunt capacitance.

The peak collector voltage $V_{\text{max}}$ and current $I_{\text{max}}$ can be determined by differentiating the
appropriate waveforms given by Eqs. (7.72) and (7.73), respectively, and setting the results
equal to zero, which gives

$$V_{\text{max}} = -2\pi\varphi V_{\text{cc}} = 3.562 V_{\text{cc}}$$
(7.74)

$$I_{\text{max}} = \left(\sqrt{\frac{\pi^2}{4} + 1}\right) I_0 = 2.8621 I_0.$$  
(7.75)

The fundamental-frequency voltage across the switch consists of two quadrature com-
ponents, whose amplitudes can be found using Fourier formulas and Eq. (7.72) as

$$V_R = -\frac{1}{\pi} \int_0^{2\pi} \frac{v(\omega t) \sin(\omega t + \varphi)}{\omega} \, d\omega t = \frac{I_R}{\pi \omega C} \left(\frac{\pi}{2} \sin 2\varphi + 2 \cos 2\varphi\right)$$
(7.76)
\[ V_L = -\frac{1}{\pi} \int_0^{2\pi} v(\omega t) \cos(\omega t + \phi) \, d\omega t = -\frac{I_r}{\pi \omega C} \left( \frac{\pi}{2} + \pi \sin^2 \phi + 2\sin 2\phi \right). \quad (7.77) \]

As a result, the optimum series inductance \( L \), shunt capacitance \( C \), and load resistance \( R \) for the supply voltage \( V_{cc} \) and fundamental-frequency output power \( P_{out} \) can be obtained by

\[ \frac{\omega L}{R} = \frac{V_L}{V_r} = 1.1525 \quad (7.78) \]

\[ \omega CR = \frac{\omega C}{I_r} V_r = 0.1836 \quad (7.79) \]

\[ R = \frac{8}{\pi^2 + 4} \frac{V_{cc}^2}{P_{out}} = 0.5768 \frac{V_{cc}^2}{P_{out}}. \quad (7.80) \]

Finally, the phase angle of the load network seen by the switch at the fundamental frequency required for an idealized optimum (or nominal) Class-E mode with shunt capacitance can be obtained through the load-network parameters using Eqs. (7.78) and (7.79) as

\[ \phi = \tan^{-1} \left( \frac{\omega L}{R} \right) - \tan^{-1} \left( 1 - \frac{\omega L}{R} \frac{\omega CR}{\omega CR} \right) = 35.945^\circ. \quad (7.81) \]

When realizing a Class-E operation mode, it is very important to know up to which maximum frequency such an idealized efficient operation mode can be extended. In this case, it is important to establish a relationship between the maximum operation frequency \( f_{\text{max}} \), shunt capacitance \( C \), output power \( P_{out} \), and supply voltage \( V_{cc} \) by using Eqs. (7.79) and (7.80) when

\[ f_{\text{max}} = 0.0507 \frac{P_{out}/CV_{cc}^2}{0.0507} \quad (7.82) \]

where \( C = C_{out} \) is the device output capacitance limiting the maximum operation frequency of an idealized optimum Class-E power amplifier with shunt capacitance.

The high-\( Q_L \) assumption for the series resonant \( L_0C_0 \) circuit can lead to considerable errors if its value is substantially small in real circuits [33]. For example, for a 50% duty ratio, the values of the load-network parameters for the loaded quality factor \( Q_L \) less than unity can differ by several tens of percentages. At the same time, for \( Q_L \geq 7 \), the errors are found to be less than 10% and they become less than 5% for \( Q_L \geq 10 \). To match the required optimum Class-E load-network resistance \( R \) with a standard load impedance \( R_L \), usually equal to 50 \( \Omega \), the series resonant \( L_0C_0 \) circuit should be followed (or fully replaced) by the matching circuit, in which the first element represents a series inductor to provide high impedance at the second and higher-order harmonics [27].
7.3.2. **Effect of saturation resistance, finite switching time, and nonlinear shunt capacitance**

In practical power amplifier design, especially when a value of the supply voltage is sufficiently small, it is very important to predict the overall degradation of power amplifier efficiency due to finite value of the transistor saturation resistance. Figure 7.30(a) shows the simplified equivalent circuit of a Class-E power amplifier with shunt capacitance, including the saturation resistance (on-resistance) $r_{\text{sat}}$ connected in series to the ideal switch. To obtain a quantitative estimate of the power losses due to the contribution of $r_{\text{sat}}$, the saturated output power $P_{\text{sat}}$ can be obtained with a simple approximation when the current $i(\omega t)$ flowing through the saturation resistance $r_{\text{sat}}$ is determined in an ideal case by Eq. (7.73).

$$P_{\text{sat}} = \frac{r_{\text{sat}}}{2\pi I_0 V_{cc}} \int_0^{\tau} i^2(\omega t) d\omega t$$  \hspace{1cm} (7.73)

where $P_0 = I_0 V_{cc}$ is the dc power. As a result, Eq. (7.73) can be rewritten as

$$\frac{P_{\text{sat}}}{P_0} = \frac{r_{\text{sat}} I_0}{2\pi V_{cc}} \frac{\pi^2}{8} \left( \frac{\pi^2}{2} + 28 \right) = \frac{r_{\text{sat}}}{2R} \frac{\pi^2}{\pi^2 + 4} = 1.365 \frac{r_{\text{sat}}}{R}. \hspace{1cm} (7.74)$$

The collector efficiency $\eta$ can be calculated from

**Fig. 7.30.** Equivalent Class-E load networks (a) with saturation resistance and (c) nonlinear capacitance and (b) current waveform with finite time delay.
Consequently, the presence of the saturation resistance results in finite value of the saturation voltage $V_{\text{sat}}$, which can be defined from

\[ V_{\text{sat}} = 1 - \frac{1}{1 + 1.365 \frac{r_{\text{sat}}}{R}} \]

(7.86)

where $V_{\text{sat}}$ is normalized to the dc supply voltage $V_{\text{cc}}$ [34].

More detailed theoretical analysis of the time-dependent behavior of the collector voltage and current waveforms shows that, for finite value of the saturation resistance $r_{\text{sat}}$, the optimum conditions for idealized operation mode given by Eqs. (7.62) and (7.63) do not correspond anymore to minimum dissipated power losses, and there are optimum nonzero values of the collector voltage and its derivative at switching time instant corresponding to minimum overall power losses [24, 35]. For example, even for small losses with the normalized loss parameter $\omega C r_{\text{sat}} = 0.1$ for a duty ratio of 50%, the optimum series inductance $L$ is almost two times greater, whereas the optimum shunt capacitance $C$ is of about 20% greater than those obtained under nominal conditions. Thus, generally the nominal switching conditions given by Eqs. (7.62) and (7.63) can be considered optimum only for idealized case of a Class-E load network with zero saturation resistance providing the switching-mode transistor operation when it operates in pinch-off and saturation regions only. However, they can be considered as a sufficiently accurate initial guess for further design and optimization in a real Class-E power amplifier design.

For an ideal transistor without any memory effects due to intrinsic phase delays, the switching time is equal to zero when the rectangular input drive results in a rectangular output response. Such an ideal case assumes zero device feedback capacitance and zero device input resistance. However, at higher frequencies, it is very difficult to realize the driving signal close to the rectangular form, as it leads to the significant circuit complexity. Fortunately, to realize high-efficiency operation conditions, it is sufficient to drive the power amplifier simply with a sinusoidal signal. The finite-time transition from the saturation mode to the pinch-off mode through the device active mode takes place due to the device inertia when the base (or channel) charge changes to zero with some finite delay time $\tau$, as shown in Fig. 7.30(b). To minimize the switching time interval, it is sufficient to slightly overdrive the transistor with a signal amplitude by 20 to 30% higher than is required for a conventional Class-B power amplifier.

The power dissipated during this on-to-off transition can be calculated assuming zero on-resistance as

\[ \eta = \frac{P_{\text{out}}}{P_0} = \frac{P_0 - P_{\text{sat}}}{P_0} = 1 - \frac{P_{\text{sat}}}{P_0}. \]  

(7.85)
\[ P_s = \frac{1}{2\pi} \int_{\varphi_s}^\pi i(\omega t) v(\omega t) \text{d}\omega t \]  
(7.87)

where the collector voltage during the transition time \( \tau_s = \pi - \varphi_s \) is defined as
\[ v(\varphi_s) = \frac{1}{\omega C} \int_{\varphi_s}^\pi i_c(\omega t) \text{d}\omega t. \]  
(7.88)

The short duration of the switching time and the proper behavior of the resulting collector (or drain) waveform allows us to make an additional assumption of a linearly decreasing collector current during fall time \( \tau_s = \pi - \varphi_s \), starting at \( i(\varphi_s) \) at time \( \varphi_s \) and decaying to zero at time \( \tau_e = \pi \) [36]. As a result, the power dissipated during transition can be then written by assuming in view of a short transition time that \( i(\varphi_s) = i(\pi) = 2I_0 \) as
\[ \frac{P_s}{P_0} = \frac{I_0 \tau_s^2}{12\pi\omega CV_c} = \frac{\tau_s^2}{12} . \]  
(7.89)

As a result, the collector efficiency \( \eta \) can be estimated as
\[ \eta = 1 - \frac{P_s}{P_0} = 1 - \frac{\tau_s^2}{12} . \]  
(7.90)

As follows from Eq. (7.89), the power losses due to nonzero switching time are sufficiently small and, for example, for \( \tau_s = 0.35 \) or \( 20^\circ \), they are only about 1%, whereas they are approximately equal to 10% for \( \tau_s = 60^\circ \). A more exact analysis assuming linear variation of the collector current during on-to-off transition produces similar results when efficiency degrades to 97.72% for \( \tau_s = 30^\circ \) and to 90.76% for \( \tau_s = 60^\circ \) [37]. Considering an exponential collector current decay rather than linear during the fall time shows similar result for \( \tau_s = 30^\circ \) when \( \eta = 96.8\% \), but the collector efficiency degrades more significantly at longer fall times when, for example, \( \eta = 86.6\% \) for \( \tau_s = 60^\circ \) [38].

In a common case, the intrinsic output device capacitance is nonlinear, as shown in Fig. 7.30(c). If its contribution in overall shunt capacitance is sufficiently large, it is necessary to consider the nonlinear nature of this capacitance when specifying the breakdown voltage. For example, the collector voltage waveform will rise in the case of the output capacitance described by abrupt diode junction in comparison with the linear capacitance, and its maximum voltage can be greater by about 20% for a 50% duty ratio [27, 39]. However, stronger nonlinearity of the shunt capacitance causes the peak voltages to be higher [40]. At the same time, the deviations of the optimum load-network parameters are insignificant, less than 5% in a wide range of supply voltages. Because the nonlinear capacitance is largest at zero voltage, the collector waveform will rise more slowly than in the linear case. As the collector voltage increases, the capacitance will decrease, and hence the voltage should begin to rise faster than in the linear
7-41

case. If the shunt capacitance consists of both nonlinear and linear capacitances, the collector voltage waveform is intermediate and located between the two extreme cases of entirely nonlinear or entirely linear capacitance [41].

7.3.3. Load network with transmission lines

The transmission lines are often preferred over lumped inductors at microwave frequencies for high-power amplifiers because of the convenience of their practical implementation, more predictable performance, less insertion loss, and less effect of the parasitic elements. For example, the matching circuit can be composed with any types of the transmission lines, including open- or short-circuit stubs, to provide the required matching and harmonic suppression conditions. In this case, to approximate the idealized Class-E operation mode of the microwave power amplifier, it is necessary to design the transmission-line load network satisfying the required idealized optimum impedances at the fundamental-frequency and harmonic components. The device output capacitance can fully represent the required shunt capacitance, whose nominal value is defined by Eq. (7.79). Consequently, the main challenge is to satisfy the idealized optimum requirements for the fundamental-frequency impedance $Z_L(\omega_0)$ shown in Fig. 7.31(a) and harmonic impedances $Z_L(n\omega_0)$ shown in Figs. 7.31(b), which can be written using Eq. (7.78) as

$$Z_L(\omega_0) = R + j\omega L = R \left( 1 + j \frac{\omega L}{R} \right) = R \left( 1 + j \tan 49.052^\circ \right)$$  \hspace{1cm} (7.91)$$

$$Z_L(n\omega_0) = \infty$$  \hspace{1cm} (7.92)

where $\omega_0$ is the fundamental angular frequency and $n \geq 2$ is the harmonic number.

![Fig. 7.31. Optimum load impedance and two-harmonic Class-E voltage waveform.](image_url)
Generally, it is practically impossible to realize these conditions for an infinite number of harmonic components by using only transmission lines. However, as it turns out from the Fourier-series analysis, a good approximation to Class-E mode may be obtained with the dc, fundamental-frequency, and second-harmonic components of the voltage waveform across the switch [42, 43]. Figure 7.31(c) shows the collector (drain) voltage waveform containing these two harmonic components (dashed curve) plotted along with an ideal voltage waveform (solid curve). In practical implementation, the two-harmonic Class-E load network designed for microwave applications will include the series microstrip line $l_1$ and open-circuit stub $l_2$, as shown in Fig. 7.32(a). The electrical lengths of microstrip lines $l_1$ and $l_2$ are chosen to be of about $45^\circ$ at the fundamental frequency to provide an open-circuit condition seen from the device output at the second harmonic, according to Eq. (7.92). Their characteristic impedances are calculated to satisfy the required inductive impedance condition at the fundamental frequency given by Eq. (7.91). However, for a packaged active device, its output lead inductance should be accounted for by shortening the length of $l_1$.

![Fig. 7.32. Equivalent circuits of Class-E power amplifiers with transmission lines.](image)

In some cases, a value of the device output capacitance exceeds the required nominal value for a Class-E mode with shunt capacitance. In this situation, it is possible to approximate Class-E mode with high efficiency by setting a properly optimized load at the fundamental frequency and strong reactive load at the second- and third-harmonic components [44]. Such a harmonic-control network consists of open-circuit quarterwave stubs at the second- and third-harmonic components separately, as shown in Fig. 7.32(b), where the third-harmonic quarterwave stub is located before the second-harmonic quarterwave stub. As a result, a very high collector efficiency can be achieved even with values of the device output capacitance higher than conventionally required at the expense of lower output power, while keeping the load at the second and third harmonics strictly inductive (inverse mode).
7.3.4. **Practical Class-E power amplifiers**

High level of output power with very high operational efficiency can be easily achieved in a Class-E mode by using high-voltage power MOSFET devices at high (HF) and very high (VHF) frequencies. Figure 7.33(a) shows the circuit schematic of a 27.12-MHz, 500-W Class-E MOSFET power amplifier with a drain efficiency of 83% at a supply voltage of 125 V [45]. The input ferrite transformer provides the 2:1 transformation voltage ratio to match the gate impedance, which is represented by the parallel equivalent circuit with a capacitance of 2200 pF and a resistance of 210 Ω. Use of the external parallel resistor of 25 Ω simplifies the matching procedure and improves the amplifier stability conditions. The transformer secondary winding provides an inductance of 19 nH, which is required to compensate for the device input capacitance at the fundamental. High-quality passive components are necessary to use in the low-pass \( L \)-type output network, where the quality factor of the bare copper wire inductor was equal to 375. The series blocking capacitor consists of three parallel disc ceramic capacitors. To realize a Class-E operation with shunt capacitance, it is sufficient to be limited to only the output device capacitance with a value of 125 pF. This is just slightly larger than that required to obtain the idealized optimum drain voltage and current Class-E waveforms.

![Circuit Schematic](image)

**Fig. 7.33.** High-power lumped Class-E power amplifiers.

Figure 7.33(b) shows the simplified circuit schematic of a silicon carbide (SiC) MESFET Class-E power amplifier that provides a maximum drain efficiency of 86.8% at an output power.
of 20.5 W at 145 MHz reached at a drain voltage of 30 V, with an input drive power level of 27 dBm [46]. The nominal Class-E impedance of approximately 18 Ω was matched to a 50-Ω load with a low-pass three-section \( L \)-type matching network to suppress harmonics by at least 60 dB below the carrier. The input of the active device was matched to 50-Ω source by means of a high-pass filter network to prevent the attenuation of the high-frequency harmonic components of the driving signal. Because this power amplifier was designed to provide linear amplification by restoring the input signal envelope with drain amplitude modulation, the drain bias network was built with a low-pass filter that allows drain modulating frequencies of up to a few megahertz to pass through it with minimum attenuation, while at the same time achieving acceptable isolation at the carrier frequency and its harmonics.

![Circuit schematic of transmission-line Class-E power amplifiers.](image)

Figure 7.34 shows the circuit schematic of a \( K \)-band transmission-line Class-E power amplifier using a single-section load network, which is well suited for monolithic implementation at upper microwave frequencies [47]. The electrical parameters of the capacitive stubs \( TL_2 \) and \( TL_3 \) were designed to provide low impedances at the second and third harmonics by making the electrical length of the stubs exactly one quarter-wavelength at a particular harmonic. At the same time, the characteristic impedances of the stubs are chosen to provide the desired capacitive reactance for load impedance transformation at the fundamental frequency. The electrical parameters of the series transmission line \( TL_1 \) are determined by the requirements to provide the optimum inductive impedance with a load angle of 49.05° at the fundamental and to transform the low impedance of the stub inputs toward higher reactances at the selected harmonics. As a result, by using a GaAs pHEMT technology and coplanar waveguides for transmission-line implementation, an output power of 20 dBm, a drain efficiency of 59%, and a power gain of 7.5 dB were achieved at an operating frequency of 24 GHz with a supply voltage of 2.4 V when both the second and third harmonics are suppressed by more than 30 and 35 dB, respectively.
7.4. **Class E with finite dc-feed inductance**

In practice, it is impossible to realize RF choke with infinite impedance at the fundamental frequency and other harmonic components. Moreover, using a finite dc-feed inductance has an advantage of minimizing size, cost, and complexity of the overall circuit. The detailed approach to analyzing the effect of a finite dc-feed inductance on the idealized Class-E mode with shunt capacitance and series filter was first described in [48]. An analysis was based on the Laplace-transform technique to solve a second-order differential equation describing the behavior of a Class-E load network with finite dc-feed inductance. Later this approach was extended to the load network with finite \( Q_L \)-factor of the series filter and finite device saturation resistance [49, 50]. However, because the results of excessive analytical and numerical calculations are given only for a few special cases, it is difficult to figure out the basic behavior of the load-network elements and derive simple equations for their parameters. Later, it was analytically shown for a 50% duty ratio based on the optimum Class-E conditions that the series excessive reactance can be either inductive or capacitive depending on the values of the dc-feed inductance and shunt capacitance [51, 52].

### 7.4.1. General analysis and optimum load-network parameters

The generalized second-order load network of a switching-mode Class E power amplifier with finite dc-feed inductance is shown in Fig. 7.35(a) [53-55]. The load network consists of a shunt capacitor \( C \), a parallel inductor \( L \), a series inductor \( L_b \), a series reactance \( X \), a series resonant \( L_0C_0 \) circuit tuned to the fundamental frequency, and a load resistance \( R \). In a common case, a shunt capacitance \( C \) can represent the intrinsic device output capacitance and external circuit capacitance added by the load network, a series inductor \( L_b \) can be considered a a bondwire and lead inductance, a parallel inductance \( L \) represents the finite dc-feed inductance, and a series reactance \( X \) can be positive (inductance), negative (capacitance), or zero depending on the certain Class-E mode. The active device is considered an ideal switch that is driven to provide the device instant switching between its on-state and off-state operation modes. To simplify an analysis of the general-circuit Class-E power amplifier, whose simplified equivalent circuit is shown in Fig. 7.35(b), it is best to introduce the preliminary assumptions similar to those for the Class-E power amplifier with shunt capacitance, assuming that the losses in the reactive circuit elements are negligible, the duty ratio is 50%, the loaded quality factor of the series \( L_0C_0 \) circuit is sufficiently high, and to set an inductance \( L_b \) to zero. For a lossless operation mode, it is necessary to provide the optimum zero-voltage and zero-voltage-derivative conditions for voltage \( v(\omega t) \) across the switch just prior to the start of switch on, when transistor is saturated, given by Eqs. (7.62) and (7.63).
Fig. 7.35. Equivalent circuits of the Class-E power amplifiers with generalized load network.

The output current flowing through the load is written as sinusoidal by

\[ i_R(\omega t) = I_R \sin(\omega t + \varphi) \]  

(7.93)

where \( I_R \) is the load current amplitude and \( \varphi \) is the initial phase shift.

When the switch is turned on for \( 0 \leq \omega t < \pi \), the voltage on the switch is \( v(\omega t) = V_{cc} - v_i(\omega t) = 0 \), the current flowing through the capacitance is \( i_C(\omega t) = \omega C (dv_L/d\omega t) = 0 \), and

\[ i(\omega t) = i_L(\omega t) + i_R(\omega t) = \frac{1}{\omega L} \int_0^{\omega t} V_{cc} d\omega t + i_L(0) + I_R \sin(\omega t + \varphi) \]

\[ = \frac{V_{cc}}{\omega L} \omega t + I_R \left[ \sin(\omega t + \varphi) - \sin \varphi \right] \]  

(7.94)

where the initial value for the current \( i_L(0) \) flowing through the dc-feed inductance \( L \) at \( \omega t = 0 \) can be found using Eq. (7.93) for \( i(0) = 0 \) as \( i_L(0) = -I_R \sin \varphi \).

When the switch is turned off for \( \pi \leq \omega t < 2\pi \), the switch current \( i(\omega t) = 0 \), and the current \( i_C(\omega t) = i_L(\omega t) + i_R(\omega t) \) flowing through the capacitance \( C \) can be rewritten as

\[ \omega C \frac{dv(\omega t)}{d\omega t} = \frac{1}{\omega L} \int_\pi^{\omega t} [V_{cc} - v(\omega t)] d\omega t + i_L(\pi) + I_R \sin(\omega t + \varphi) \]  

(7.95)

under the initial off-state conditions \( v(\pi) = 0 \) and

\[ i_L(\pi) = i(\pi) - i_R(\pi) = \frac{V_{cc} \pi}{\omega L} - \omega L I_R \sin \varphi. \]

Equation (7.95) can be represented in the form of the linear nonhomogeneous second-order differential equation

\[ \omega^2 LC \frac{d^2 v(\omega t)}{d(\omega t)^2} + v(\omega t) - V_{cc} - \omega L I_R \cos(\omega t + \varphi) = 0 \]  

(7.96)

the general solution of which can be obtained in the normalized form
\[
\frac{v(\omega t)}{V_{cc}} = C_1 \cos(\omega t) + C_2 \sin(\omega t) + 1 - \frac{q^2 p}{1 - q^2} \cos(\omega t + \varphi) \tag{7.97}
\]

where
\[
q = \frac{1}{\omega \sqrt{LC}} \tag{7.98}
\]
\[
p = \frac{\omega L I_R}{V_{cc}} \tag{7.99}
\]

and the coefficients \(C_1\) and \(C_2\) are determined from the initial off-state conditions [36].

The dc supply current \(I_0\) can be found using Fourier formula and Eq. (7.94) by
\[
I_0 = \frac{1}{2\pi} \int_0^{2\pi} i(\omega t) \, d\omega t = \frac{I_R}{2\pi} \left( \frac{\pi^2}{2p} + 2\cos\varphi - \pi \sin\varphi \right). \tag{7.100}
\]

In an idealized Class-E operation mode, there is no nonzero voltage and current simultaneously that means a lack of power losses and gives an idealized collector efficiency of 100%. This implies that the dc power \(P_0\) and fundamental output power \(P_{out}\) are equal,
\[
I_0 V_{cc} = \frac{V_R^2}{2R} \tag{7.101}
\]
where \(V_R = I_R R\) is the fundamental voltage amplitude across the load resistance \(R\).

As a result, by using Eqs. (7.100) and (7.101) and considering that \(R = V_R^2/2P_{out}\), the optimum load resistance \(R\) for the specified values of a supply voltage \(V_{cc}\) and fundamental output power \(P_{out}\) can be obtained by
\[
R = \frac{1}{2} \left( \frac{V_R}{V_{cc}} \right)^2 \frac{V_{cc}^2}{P_{out}} \tag{7.102}
\]

where
\[
\frac{V_R}{V_{cc}} = \frac{1}{\pi} \left( \frac{\pi^2}{2p} + 2\cos\varphi - \pi \sin\varphi \right). \tag{7.103}
\]

The normalized load-network inductance \(L\) and capacitance \(C\) can be appropriately defined using Eqs. (7.98) through (7.100) as
\[
\omega L \frac{R}{R} = p I \left( \frac{\pi}{2p} + \frac{2}{\pi} \cos\varphi - \sin\varphi \right) \tag{7.104}
\]
\[
\omega CR = \frac{1}{q^2} \left( \frac{\omega L \frac{R}{R}}{2} \right). \tag{7.105}
\]

The series reactance \(X\), which may have an inductive, capacitive, or zero reactance in special cases depending on the load-network parameters, can be generally calculated using two quadrature fundamental-frequency voltage Fourier components.
7-48

\[ V_R = -\frac{1}{\pi} \int_{0}^{2\pi} v(\omega t) \sin(\omega t + \varphi) \, d\omega t \]  \hspace{1cm} (7.106)

\[ V_X = -\frac{1}{\pi} \int_{0}^{2\pi} v(\omega t) \cos(\omega t + \varphi) \, d\omega t . \]  \hspace{1cm} (7.107)

The fundamental-frequency current flowing through the switch consists of two quadrature components, whose amplitudes can be found using Fourier formulas and Eq. (7.94) by

\[ I_R = \frac{1}{\pi} \int_{0}^{2\pi} i(\omega t) \sin(\omega t + \varphi) \, d\omega t \]

\[ = \frac{I_R}{\pi} \left[ \frac{\pi \cos \varphi - 2 \sin \varphi}{p} + \frac{\pi}{2} - \sin 2\varphi \right] \]  \hspace{1cm} (7.108)

\[ I_X = -\frac{1}{\pi} \int_{0}^{2\pi} i(\omega t) \cos(\omega t + \varphi) \, d\omega t \]

\[ = \frac{I_R}{\pi} \left[ \frac{\pi \sin \varphi + 2 \cos \varphi}{p} - 2 \sin^2 \varphi \right]. \]  \hspace{1cm} (7.109)

Generally, Eq. (7.97) for normalized collector voltage contains three unknown parameters \( q \), \( p \), and \( \varphi \), which must be analytically or numerically determined. In a common case, the parameter \( q \) can be considered a variable, and the other two parameters \( p \) and \( \varphi \) are calculated from a system of two equations resulting from applying two optimum zero-voltage and zero-voltage derivative conditions given by Eq. (7.62) and (7.63) to Eq. (7.97). Figure 7.36 shows the dependences of the optimum parameters \( p \) and \( \varphi \) versus \( q \) for a Class E with finite dc-feed inductance.

![Fig. 7.36. Optimum Class-E parameters \( p \) and \( \varphi \) versus \( q \).](image_url)
Based on the calculated optimum parameters $\rho$ and $\varphi$ as functions of $q$, the optimum load-network parameters of the Class-E load network with finite dc-feed inductance can be determined using Eqs. (7.102) through (7.105). The series reactance $X$ can be calculated by the ratio of two quadrature fundamental-frequency voltage Fourier components given in Eqs. (7.106) and (7.107) as

$$\frac{X}{R} = \frac{V_X}{V_R}.$$  \hspace{1cm} (7.110)

Fig. 7.37. Normalized optimum Class-E load network parameters.

The dependences of the normalized optimum dc-feed inductance $\omega L/R$ and series reactance $X/R$ are shown in Fig. 7.37(a), whereas the dependences of the normalized optimum shunt capacitance $\omega CR$ and load resistance $R_{out}/V^2_{cc}$ are plotted in Fig. 7.37(b). Here, the value of the series reactance $X$ changes its sign from positive to negative, which means that the inductive reactance is followed by the capacitive reactance. As a result, there is a special case of the load network with a parallel circuit and a load resistor only when $X = 0$ at $q = 1.412$. In this case, the maximum value of the optimum load resistance $R$ can be provided for the same supply voltage.
and output power, thus simplifying the matching with the standard load of 50 Ω. In addition, the values of a dc-feed inductance $L$ become sufficiently small, making Class-E mode with a parallel circuit very attractive for monolithic applications. The maximum operation frequency $f_{\text{max}}$ is realized at $q = 1.468$, where the normalized optimum shunt capacitance $\omega CR$ reaches its maximum.

### 7.4.2. Parallel-circuit Class E

The theoretical analysis of a switching-mode parallel-circuit Class-E power amplifier with a series filter, whose basic circuit schematic is shown in Fig. 7.38(a), was first published by Kozyrev with calculation of the voltage and current waveforms and some graphical results [27, 56]. The load network consists of a finite dc-feed inductor $L$, a shunt capacitor $C$, a series $L_0C_0$ resonant circuit tuned to the fundamental frequency, and a load resistor $R$. In this case, the switch sees a parallel connection of the load resistor $R$ and parallel $LC$ circuit at the fundamental frequency, as shown in Fig. 7.38(b), where also the real and imaginary collector fundamental-frequency current components $I_X$ and $I_R$ and the real collector fundamental-frequency voltage component $V_R$ are indicated.

![Fig. 7.38. Equivalent circuits of parallel-circuit Class-E power amplifier.](image)

In the case of a parallel-circuit Class-E load network without series phase-shifting reactance, because the parameter $q$ is unknown a priori, generally it is necessary to solve a system of three equations to define the three unknown parameters $q$, $p$, and $\phi$. The first two equations are the result of applying two optimum zero-voltage and zero-voltage-derivative conditions given by Eq. (7.62) and (7.63) to Eq. (7.97). Because the fundamental-frequency collector voltage is fully applied to the load, this means that its reactive part must have zero value, resulting in an additional equation.
$$V_x = -\frac{1}{\pi} \int_{0}^{2\pi} v(\omega t) \cos(\omega t + \phi) d\omega t = 0. \quad (7.111)$$

Solving the system of three equations with three unknown parameters numerically gives the following values [57, 58]:

$$q = 1.412 \quad (7.112)$$

$$p = 1.210 \quad (7.113)$$

$$\phi = 15.155^\circ. \quad (7.114)$$

Figure 7.39 shows the normalized (a) load current and collector (b) voltage, and (c) current waveforms for an idealized optimum parallel-circuit Class-E operation mode. From collector voltage and current waveforms, it follows that, like other Class-E subclasses, there is no nonzero voltage and current simultaneously. When this happens, no power loss occurs and an idealized collector efficiency of 100% is achieved.

![Figure 7.39](image)

Fig. 7.39. Normalized (a) load current and collector (b) voltage and (c) current waveforms for idealized optimum parallel-circuit Class E.

By using Eqs. (7.102) through (7.105), the idealized optimum (or nominal) load resistance $R$, parallel inductance $L$, and parallel capacitance $C$ can be appropriately obtained by
\[ R = 1.365 \frac{V_{cc}^2}{P_{out}} \]  \hspace{1cm} (7.115)

\[ L = 0.732 \frac{R}{\omega} \]  \hspace{1cm} (7.116)

\[ C = \frac{0.685}{\omega R} . \]  \hspace{1cm} (7.117)

The dc supply current \( I_0 \) can be calculated from Eq. (7.100) as
\[ I_0 = 0.826 I_R . \]  \hspace{1cm} (7.118)

The phase angle \( \phi \) seen from the device collector at the fundamental frequency can be represented either through two fundamental-frequency current quadrature Fourier components \( I_x \) and \( I_y \) given by Eqs. (7.108) and (7.109) or as a function of the load-network elements by
\[ \phi = \tan^{-1} \left( \frac{R}{\omega L} - \omega RC \right) = 34.244^\circ. \]  \hspace{1cm} (7.119)

If the calculated value of the optimum Class-E load resistance \( R \) is too small or differs significantly from the standard load impedance (usually equal to 50 \( \Omega \)), it is necessary to use an additional matching circuit to deliver maximum output power to the load. It should be noted that, among a family of the Class-E load networks, a parallel-circuit Class-E load network offers the largest value of \( R \), thus simplifying the final matching design procedure. In this case, the first series element of such matching circuits should be the inductor to provide high impedance conditions for harmonics, as shown in Fig. 7.40.

![Fig. 7.40](image)

The peak collector current \( I_{\text{max}} \) and peak collector voltage \( V_{\text{max}} \) can be determined from Eqs. (7.94), (7.97), and (7.118) as
\[ I_{\text{max}} = 2.647 I_0 \]  \hspace{1cm} (7.120)

\[ V_{\text{max}} = 3.647 V_{cc} . \]  \hspace{1cm} (7.121)

The maximum frequency \( f_{\text{max}} \) can be calculated using Eq. (7.115) and (7.117) when \( C = C_{\text{out}} \), where \( C_{\text{out}} \) is the device output capacitance, as
which is 1.57 times higher than the maximum operation frequency for an optimum Class-E power amplifier with shunt capacitance given by Eq. (7.82).

### 7.4.3. Even-harmonic Class E

The well-defined analytic solution based on an assumption of the even-harmonic resonant conditions when the finite dc-feed inductance and parallel capacitance are tuned to any even-harmonic component was given in [59]. The load network of an even-harmonic Class E is shown in Fig. 7.41, where the series capacitor $C_X$ is needed to compensate for the excessive inductive reactance caused by the preliminary choice of the specified load-network parameters. The value of this capacitance can be found from the consideration of two fundamental-frequency voltage quadrature components across the switch given by Eqs. (7.106) and (7.107).

![Fig. 7.41. Equivalent circuit of the even-harmonic Class-E power amplifier.](image)

Since, for an even-harmonic Class-E operation mode, the dc-feed inductance is restricted to values that satisfy an even-harmonic resonance condition and it is assumed the fundamental-frequency voltage across the switch and output voltage across the load have a phase difference of $\pi/2$, the two unknown parameters can be set in this specified case as

\[
q = 2n \quad (7.123)
\]

\[
\phi = -90^\circ \quad (7.124)
\]

where $n = 1, 2, 3, \ldots$

The third parameter $p$ can be found using an idealized optimum zero voltage-derivative condition given by Eq. (7.63) as

\[
p = \frac{4n^2 - 1}{8n^2 - \pi} \quad (7.125)
\]

The dc supply current $I_0$ can be found from Eq. (7.100) by

\[
I_0 = \frac{1}{2\pi} \int_0^{2\pi} \frac{i(\omega t)}{2(4n^2 - 1)} I_\pi \quad (7.126)
\]
As a result, the normalized steady-state collector voltage waveform for $\pi \leq \omega t < 2\pi$ and current waveform for period of $0 \leq \omega t < \pi$ are

$$\frac{v(\omega t)}{V_{cc}} = 1 - \frac{\pi}{2} \sin \omega t + \frac{\pi}{4n} \sin(2n\omega t) - \cos(2n\omega t)$$  \hspace{1cm} (7.127)$$

$$\frac{i(\omega t)}{I_0} = 2 \left[ \frac{8n^2}{\pi} \omega t - 4n^2 + 1 + (4n^2 - 1) \cos \omega t \right].$$  \hspace{1cm} (7.128)$$

![Graphs of the waveforms](image)

Fig. 7.42. Normalized (a) load current and collector (b) voltage and (c) current waveforms for idealized optimum even-harmonic Class E.

Figure 7.42 shows the normalized (a) load current, (b) collector voltage, and (c) collector current waveforms for an idealized optimum even-harmonic Class-E mode. If the collector voltage waveform corresponding to even-harmonic Class E is very similar to the collector voltage waveform corresponding to Class E with shunt capacitance, then the behavior of the collector current waveform is substantially different. For even-harmonic Class-E configuration, the collector current reaches its peak value, which is four times as high as the dc current, at the end of
the conduction interval. Consequently, in the case of a sinusoidal driving signal it is impossible to provide close to the maximum collector current when the input base current is smoothly reducing to zero.

The optimum load-network parameters for the most practical case when \( n = 1 \) can be calculated from

\[
R = \frac{1}{18} \frac{V_{cc}^2}{P_{out}} = 0.056 \frac{V_{cc}^2}{P_{out}} \tag{7.129}
\]

\[
L = \frac{9\pi R}{8 \omega} = 3.534 \frac{R}{\omega} \tag{7.130}
\]

\[
C = \frac{2}{9\pi} \frac{1}{\omega R} = 0.071 \frac{1}{\omega R} \tag{7.131}
\]

\[
C_X = \frac{4\pi}{32 + 3\pi^2} \frac{1}{\omega R} = 0.204 \frac{1}{\omega R} \tag{7.132}
\]

The main problem of an even-harmonic Class-E operation mode is a substantially small value of the load resistance \( R \), which is over an order of magnitude smaller than for a Class E with shunt capacitance and much smaller than for a parallel-circuit Class E.

The phase angle \( \phi \) between the fundamental-frequency voltage and current components seen by switch is equal to

\[
\phi = \frac{3}{4} \frac{R}{\omega L} \left( 1 + \left( \frac{\omega C_X R}{R} \right)^2 \right) - \frac{1}{\omega C_X R} = 22.302^\circ \tag{7.133}
\]

whereas the maximum frequency \( f_{max} \), up to which an idealized optimum even-harmonic Class-E mode can be realized, is calculated from

\[
f_{max} = \frac{2}{\pi^2} \frac{P_{out}}{C_{out} V_{cc}^2} = 0.203 \frac{P_{out}}{C_{out} V_{cc}^2} \tag{7.134}
\]

where \( C_{out} \) is the device output capacitance.

### 7.4.4. Load networks with transmission lines

At microwave frequencies, the parallel inductance \( L \) can be replaced by a short-length short-circuited transmission line \( TL \) according to

\[
Z_0 \tan \theta = \omega L \tag{7.135}
\]

where \( Z_0 \) and \( \theta \) are the characteristic impedance and electrical length of such a transmission line, respectively [60]. By using Eq. (7.116) defining the idealized optimum (or nominal) parallel inductance \( L \) for a parallel-circuit Class-E mode, Eq. (7.135) can be rewritten as

\[
tan \theta = 0.732 \frac{R}{Z_0}. \tag{7.136}
\]
Generally, the load-network circuit can be composed with any types of transmission lines, including open-circuit or short-circuit stubs to provide the required matching and harmonic-suppression conditions. In some cases, for example, for compact small-size power-amplifier modules designed for handset or small-cell wireless transmitters, the series microstrip lines and shunt chip capacitors are usually used in the external output matching circuits. However, to maintain the optimum-switching conditions at the fundamental frequency, such an output matching circuit should contain the series transmission line as the first element.

![Fig. 7.43. Transmission-line load network of parallel-circuit Class-E power amplifier for handset application.](image)

Figure 7.43(a) shows an example of the transmission-line Class-E load network of a two-stage 1.75-GHz GaAs HBT power amplifier with an output power of 33 dBm, which was designed for a cellular handset transmitter, and includes the series microstrip line with two shunt chip capacitors [57]. However, because of the fixed electrical lengths of the transmission lines, it is impossible to realize simultaneously the required inductive impedance at the fundamental frequency with the purely capacitive reactances at higher-order harmonics. For example, at the second harmonic, the real part of the load network impedance \( Z_{\text{net}}(2\omega_0) \) is sufficiently high, as shown in Fig. 7.43(b). Nevertheless, even such an approximation provides a good proximity to the parallel-circuit Class-E operation mode, resulting in a high operating efficiency of the power amplifier. In this case, there is no need to use an additional RF choke for dc supply current, because its function can be performed by the same short-length parallel microstrip line required to provide an optimum inductive impedance at the fundamental frequency.

The circuit schematic of a two-stage InGaP/GaAs HBT power amplifier intended to operate in the WCDMA handset transmitters is shown in Fig. 7.44(a) [61]. The MMIC part of this power amplifier contains the transistors with emitter areas of the first and second stage as
large as 540 $\mu$m$^2$ and 3600 $\mu$m$^2$, input matching circuit, interstage matching circuit, and bias circuits on a die with overall dimension of less than 1 mm$^2$. The broadband capability of the PA was verified with regard to the DCS1800 and PCS1900 frequency bands. Without any tuning of the output matching circuit, a saturated output power greater than 30 dBm and a $PAE$ greater than 50% were obtained. Using high-$Q$ capacitors in output matching circuit can improve the power-added efficiency by about 8%. The power gain of 22.5±0.5 dB and the input return loss greater than 13 dB were measured from 1.6 GHz to higher than 2 GHz. At the same time, this power amplifier without any additional tuning could provide the high-linearity performance for WCDMA band (1920-1980 MHz) at a 3.5-dB backoff output power of 27 dBm with a power gain of 22.6 dB and a sufficiently high efficiency. The measured $PAE$ reached value of 38.3% at center bandwidth frequency of 1.95 GHz with an adjacent channel leakage power ratio ($ACLR$) of –37 dBc at a 5-MHz offset.

![Schematics of Class-E power amplifiers with transmission-line matching.](image)

**Fig. 7.44.** Schematics of Class-E power amplifiers with transmission-line matching.

Figure 7.44(b) shows the circuit schematic of a 1-GHz 12-V LDMOSFET parallel-circuit Class-E power amplifier with a drain efficiency of 70.4% and an output power of more than 38
dBm [62]. In this case, the series $LC$ resonant circuit is replaced by a low-pass $L$-type output matching circuit with a series transmission line to match the low optimum Class-E resistance to a 50-Ω load, having almost zero series excessive reactance $X$. The quarterwave transmission line in the gate bias circuit provides RF isolation from the dc-voltage supply, and the 12-Ω gate resistor is required for stability reason.

### 7.5. Class E with shunt capacitance and shunt filter

Class E with shunt capacitance and shunt filter represents an alternative to Class E with shunt capacitance and series filter when high loaded quality of the shunt filter is provided by higher value capacitance rather than inductance, thus making such a Class-E power amplifier more compact when no need to use high-value inductors in both dc-supply and resonant circuits. In this case, much better harmonic suppression can be achieved by using a high-$Q$ shunt filter with a low-value shunt capacitance. The theoretical analysis and practical implementation of a vacuum-tube Class-E amplifier with shunt filter was first provided in late 1960s [24]. This circuit was analyzed by solving the second-order differential equation for voltage across shunt capacitor but the final design equations for the load-network parameters were not derived in explicit form. The anode voltage and current waveforms were analytically derived and numerically calculated for the specific case of $q = 2$.

#### 7.5.1. Basic analysis and optimum load-network parameters

The optimum parameters of a single-ended Class-E power amplifier with shunt capacitance and shunt filter can be determined based on an analytical derivation of its steady-state collector voltage and current waveforms. Figure 7.45(a) shows the basic circuit configuration of a Class-E power amplifier with shunt capacitance and shunt filter, where the load network consists of a shunt capacitor $C$, a series inductor $L$, a blocking capacitor $C_b$, a shunt fundamentally tuned $L_0C_0$ circuit, and a load resistor $R$ [63, 64]. In this case, the shunt $L_0C_0$ circuit operates as a harmonic filter creating zero impedance at the second- and higher-order harmonics instead of the open-circuit harmonic conditions corresponding to classical Class-E power amplifier with shunt capacitance and series filter. In a common case, a shunt capacitance $C$ can represent the intrinsic device output capacitance and external circuit capacitance added by the load network. The dc power supply is generally connected by an RF choke with infinite reactance at the fundamental and any higher-order harmonic component. The active device is considered an ideal switch that is driven at the operating frequency to provide instantaneous switching between its on-state and off-state operation conditions.
To simplify the analysis of a Class-E power amplifier with shunt filter, whose equivalent circuit is shown in Fig. 7.45(b), the following several assumptions are introduced:

- the transistor has zero saturation voltage, zero saturation resistance, infinite off-resistance, and its switching is instantaneous and lossless
- the shunt capacitance is assumed to be constant
- the shunt \(L_0C_0\) filter has zero impedance at the second- and higher-order harmonics
- there is no loss in the circuit except the load \(R\)
- for simplicity, a 50% duty ratio is used.

For idealized lossless operation mode, it is necessary to provide the zero-voltage and zero-voltage-derivative conditions for voltage across the switch (just prior to the start of switch on) at the instant \(\omega t = 2\pi\), when transistor is saturated. Then, expressions for the collector current \((0 \leq \omega t < \pi)\) and voltage \((\pi \leq \omega t < 2\pi)\) for ideal \(L_0C_0\)-circuit tuned to the fundamental frequency when the sinusoidal current \(i_R = I_R \sin(\omega t + \phi)\) flows into the load can be written as

\[
i(\omega t) = i_L(\omega t) = \frac{V_{cc}}{\omega L} \omega t + \frac{V_R}{\omega L} \left[ \cos(\omega t + \phi) - \cos \phi \right] \quad (7.137)
\]

\[
\omega^2 LC \frac{d^2 v(\omega t)}{d(\omega t)^2} + v(\omega t) - V_{cc} + V_R \sin(\omega t + \phi) = 0 \quad (7.138)
\]

where \(\phi\) is the initial phase shift and \(V_R = I_R R\) is the voltage amplitude across the load resistance \(R\) [63].

The general solution of Eq. (7.138) can be given in the normalized form as

\[
\frac{V(\omega t)}{V_{cc}} = C_1 \cos q \omega t + C_2 \sin q \omega t + 1 + \frac{q^2}{1 - q^2 V_{cc}} V_R \sin(\omega t + \phi) \quad (7.139)
\]
where $q = 1/\omega \sqrt{L/C}$ and the coefficients $C_1$ and $C_2$ are determined from the initial off-state conditions. The fundamental-frequency voltage across the switch consists of two quadrature components with an amplitude of the real component defined by Fourier formula as

$$V_R = -\frac{1}{\pi} \int_0^{2\pi} v(\omega t) \sin(\omega t + \phi) d\omega t. \quad (7.140)$$

As a result, by solving a system of three equations – two of them defined by the Class-E switching conditions given by Eqs. (7.62) and (7.63) and the third one for $V_R$ given by (7.140) – the three unknown parameters can be calculated as

$$\phi = -41.614^\circ \quad (7.141)$$
$$q = 1.607 \quad (7.142)$$
$$\frac{V_R}{V_{cc}} = 0.9253. \quad (7.143)$$

The dc current $I_0$ can be determined by applying a Fourier-series expansion to Eq. (7.137). Then, the optimum normalized series inductance $L$ and shunt capacitance $C$ can be defined using Eqs. (7.141) through (7.143) and assuming an idealized collector efficiency of 100% given by Eq. (7.101) as

$$L = 1.4836 \frac{R}{\omega} \quad (7.144)$$
$$C = \frac{0.261}{\omega R} \quad (7.145)$$

whereas the optimum load resistance $R$ can be obtained for the given supply voltage $V_{cc}$ and fundamental output power $P_{out}$ by

$$R = \frac{1}{2} \frac{V_R^2}{P_{out}} = \frac{1}{2} \left( \frac{V_R}{V_{cc}} \right)^2 \frac{V_{cc}^2}{P_{out}} = 0.4281 \frac{V_{cc}^2}{P_{out}}. \quad (7.146)$$

Figure 7.46 shows the normalized collector (a) voltage and (b) current waveforms for idealized optimum Class-E mode with shunt filter during the entire interval $0 \leq \omega t \leq 2\pi$. From the collector voltage and current waveforms, it follows that, when the transistor is turned on, there is no voltage across the switch and the current from the inductor flows through the switch. However, when the transistor is turned off, this current flows through the capacitor $C$. In this case, there is no nonzero voltage and current simultaneously, which means a lack of the power losses that gives an idealized collector efficiency of 100%.
The phase angle $\phi$ of the load network at fundamental seen by the switch which is required for an idealized optimum (or nominal) Class-E mode with shunt capacitance and shunt filter can be determined through the load-network parameters using Eqs. (7.144) and (7.145) as

$$\phi = \tan^{-1}\left(\frac{\omega L}{R}\right) - \tan^{-1}\left(\frac{\omega CR}{1 - \frac{\omega L}{R} \omega CR}\right) = 32.945^\circ$$  \hspace{1cm} (7.147)

The peak collector voltage $V_{\text{max}}$ and current $I_{\text{max}}$ are defined as

$$\frac{V_{\text{max}}}{V_{cc}} = 3.677$$ \hspace{1cm} (7.148)$$
$$\frac{I_{\text{max}}}{I_0} = 2.768$$ \hspace{1cm} (7.149)

that shows that the voltage peak factor is as high as in classical Class E with shunt capacitance and series filter [36].

In Table 7.2, the optimum impedances seen by the device collector at the fundamental-frequency and higher-order odd and even harmonic components are illustrated by the appropriate circuit configurations. As it is seen, Class-E mode with shunt capacitance and shunt filter shows different impedance properties from other alternative Class-E load networks. At even harmonics, its optimum impedances can be established by the parallel $LC$ circuit, similarly to Class E with quarterwave line and series filter. However, at odd harmonics, the optimum impedances for Class E with shunt capacitance and shunt filter differ from Class E with series
filter and Class E with quarterwave line where impedances are defined by the shunt capacitances, because they are also provided by the parallel $LC$ circuits.

Table 7.2. Optimum impedances at fundamental and harmonics.

<table>
<thead>
<tr>
<th>Class-E load network</th>
<th>$f_0$ (fundamental)</th>
<th>$2nf_0$ (even harmonics)</th>
<th>$(2n+1)f_0$ (odd harmonics)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class E with shunt capacitance and series filter</td>
<td><img src="image1" alt="Network" /></td>
<td><img src="image2" alt="Network" /></td>
<td><img src="image3" alt="Network" /></td>
</tr>
<tr>
<td>Class E with quarterwave line and series filter [36]</td>
<td><img src="image4" alt="Network" /></td>
<td><img src="image5" alt="Network" /></td>
<td><img src="image6" alt="Network" /></td>
</tr>
<tr>
<td>Class E with shunt capacitance and shunt filter</td>
<td><img src="image7" alt="Network" /></td>
<td><img src="image8" alt="Network" /></td>
<td><img src="image9" alt="Network" /></td>
</tr>
</tbody>
</table>

Table 7.3. Load-network parameters for different Class-E modes.

<table>
<thead>
<tr>
<th>Normalized load-network parameter</th>
<th>Class E with shunt capacitance and series filter</th>
<th>Class E with quarterwave line and series filter [36]</th>
<th>Class E with shunt capacitance and shunt filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{\omega L}{R}$</td>
<td>1.1525</td>
<td>1.349</td>
<td>1.4836</td>
</tr>
<tr>
<td>$\omega CR$</td>
<td>0.1836</td>
<td>0.2725</td>
<td>0.261</td>
</tr>
<tr>
<td>$\frac{P_{out}R}{V_{cc}^2}$</td>
<td>0.5768</td>
<td>0.465</td>
<td>0.4281</td>
</tr>
<tr>
<td>$\frac{f_{max}C_{out}V_{cc}^2}{P_{out}}$</td>
<td>0.0507</td>
<td>0.093</td>
<td>0.097</td>
</tr>
</tbody>
</table>

The optimized load-network parameters of the different Class-E modes including Class E with series filter, Class E with quarterwave line, and Class E with shunt filter are shown in Table 7.3 in a normalized form. As can be seen, Class E with shunt filter offers the larger value of the shunt capacitance $C$ for the same load $R$ and much higher value of the maximum operating frequency $f_{max}$ for the same dc supply voltage $V_{cc}$, device output capacitance $C_{out}$, and output power $P_{out}$, compared to Class E with shunt capacitance and series filter. At the same time, difference between Class E with quarterwave line and Class E with shunt filter is not so significant because the quarterwave line being grounded at its end through bypass capacitor operates for even harmonics as a shunt filter.
Note that generally the shunt capacitance can differ from its nominal Class-E value defined by Eq. (7.145) at high operating frequencies because the value of the device output capacitance is too large. To compensate for the excess capacitance, need to add an additional reactive element between the shunt filter and the load resistance, similar to Class E with finite dc-feed inductance. An example of such a Class-E load network with an additional reactance where the value of the circuit parameter $q$ is smaller than its nominal value given by Eq. (7.142) was analyzed in [65]. In this case, a shunt capacitance with optimum value was connected in parallel to the load resistance.

### 7.5.2. Load network with transmission lines

Figure 7.47 shows the circuit schematic of a high-efficiency Class-E power amplifier with transmission-line shunt filter and output matching circuit, where the nominal load resistance $R = \text{Re}Z_{\text{net}}(\omega_0)$ is matched to the standard load impedance $R_L = 50\,\Omega$ at the fundamental frequency using an output transmission-line $L$-type impedance transformer. Here, the shunt harmonic filter is composed of $45^\circ$ short-circuit and open-circuit stubs to create short-circuited conditions at even harmonics. To create a short-circuited condition at the third harmonic at the right-hand side of the series inductor represented by a short-length series transmission line with the characteristic impedance $Z_0$ and electrical length $\theta$, the series transmission line with electrical length of $60^\circ$ and an open-circuit stub with electrical length of $30^\circ$ are used.

For electrical length of a sufficiently short series transmission line with the characteristic impedance $Z_0$ and electrical length $\theta$ of less than $45^\circ$, the required optimum value of $\theta$ for Class-E mode with shunt capacitance and shunt filter using (7.144) can be approximated by

$$\theta = \tan^{-1}\left(1.4836 \frac{R}{Z_0}\right). \quad (7.150)$$
The output matching circuit is necessary to match to the required optimum Class-E resistance $R$ calculated in accordance with (7.146) to the standard load resistance of 50 $\Omega$. In addition, it is required to provide a short-circuit condition at the third harmonic component. This can be easily done using the output matching topology in the form of an $L$-type transformer with the series transmission line and open-circuit stub. Its load-network impedance $Z_{\text{net}}$ at the fundamental can be written as

$$Z_{\text{net}} = Z_1 \frac{R_L \left(Z_2 - Z_1 \tan 30^\circ \tan 60^\circ \right) + jZ_1 Z_2 \tan 60^\circ}{Z_1 Z_2 + j \left(Z_1 \tan 30^\circ + Z_2 \tan 60^\circ \right) R_L}$$

(7.151)

where $Z_1$ and $Z_2$ are the characteristic impedances of the series transmission line and shunt open-circuit stub, respectively.

Consequently, the complex-conjugate matching with the load at the fundamental can be provided by proper choice of the characteristic impedances $Z_1$ and $Z_2$. Separating Eq. (7.151) into real and imaginary parts and considering that $\text{Re}Z_{\text{net}} = R$ and $\text{Im}Z_{\text{net}} = 0$, the system of two equations with two unknown parameters can be written as

$$\left( Z_1 + 3Z_2 \right)^2 R_L^2 R - 3Z_1^2 Z_2^2 \left[ 4R_L - 3R \right] = 0$$

(7.152)

$$3Z_1^2 Z_2^2 + R_L^2 \left( Z_1 + 3Z_2 \right) \left( Z_2 - Z_1 \right) = 0$$

(7.153)

which enables the characteristic impedances $Z_1$ and $Z_2$ to be properly calculated.

This system of two equations can be explicitly solved as a function of the parameter $r = R_L/R$, resulting in

$$\frac{Z_1}{R_L} = \frac{\sqrt{4r - 1}}{\sqrt{3r}}$$

(7.154)

$$\frac{Z_1}{Z_2} = \frac{r - 1}{r}$$

(7.155)

As a result, for specified value of the parameter $r$ with the required optimum load resistance $R$, corresponding to Class E with shunt capacitance and shunt filter, and standard load $R_L = 50 \Omega$, first the characteristic impedance $Z_1$ is calculated from (7.154) and then the characteristic impedance $Z_2$ is calculated from (7.155). For example, if the required optimum load resistance is equal to $R = 20 \Omega$, resulting in $r = 2.5$, the characteristic impedance of the series transmission line is equal to $Z_1 = 35 \Omega$ and the characteristic impedance of the open-circuit stub is equal to $Z_2 = 58 \Omega$.

7.5.3. Design example of transmission-line Class-E power amplifier

Figure 7.48 shows the simulated circuit schematic, which approximates the transmission-line Class-E power amplifier with shunt filter and based on a 28-V 10-W Cree GaN HEMT power transistor CGH40010F and transmission-line load network including a shunt filter and a
transmission-line matching section. The input matching circuit provides a complex-conjugate matching with the standard 50-Ω source. The load network was slightly modified by optimizing the parameters of the series and shunt transmission lines because the device output capacitance $C_{\text{out}}$ and series inductance $L_{\text{out}}$ formed by drain bondwires and package lead do not match the required exact values of $C$ and $L$ for a nominal Class-E mode with shunt filter.

![Fig. 7.48. Circuit schematic of transmission-line Class-E GaN HEMT power amplifier with shunt filter.](image)

For the transmission-line GaN HEMT Class-E power amplifier with shunt filter using a 30-mil RO4350 substrate, the simulated drain efficiency of 83%, a $\text{PAE}$ of 80.4%, and a power gain of 15 dB at an output power of 40.3 dBm with a quiescent current of 30 mA are achieved at an operating frequency of 2.14 GHz with a supply voltage of 28 V, as shown in Fig. 8. The second and third harmonics were suppressed by greater than 50 dB.

![Fig. 7.49. Simulated results of transmission-line Class-E GaN HEMT power amplifier with shunt filter.](image)

### 7.6. Biharmonic Class-$E_M$ power amplifier

A basic limitation of a Class-E operation mode at higher frequencies is significant efficiency degradation due to the increased switching power losses with increasing values of the
turn-off switching time. To minimize this undesirable effect, it is necessary to find a solution without instant jump in an ideal collector current waveform at turn-off to allow efficient operation at frequencies high enough that the switch turn-off transition would occupy a substantial fraction of the waveform period, of 30% and more. However, the Class-E power amplifier can deliver nonzero output power only if at least one of the switch waveforms, either voltage or current, has a jump under assumption that the circuit comprises an ideal switch and linear passive components [32]. To satisfy the requirements of both jumpless voltage and current waveforms and sinusoidal load waveform with nonzero output power delivered to the load, it is necessary to allow power flow in the system at two or more harmonically related frequencies. This can be done by using nonlinear reactive elements in the load network to convert the fundamental-frequency power to a desired harmonic frequency or by injecting the harmonic-frequency power into the load network from an external source.

The simplest low-order implementation approach having jumpless switch voltage and current waveforms, called the biharmonic Class-EM mode and described in [66], comprises the two-part output stage including

- main amplifier that consumes dc power equal to approximately 75% of the load power and converts this power and the power generated by the auxiliary amplifier to power at the output frequency $f$
- smaller auxiliary amplifier (or varactor frequency multiplier) phased locked to the main amplifier, which generates approximately 25% of the load power at the frequency $2f$.

The main amplifier has jumpless switch voltage and current waveforms, whereas the auxiliary amplifier can be a conventional Class-E power amplifier. If the frequency multiplier is fed from the output of the main amplifier, the load power is reduced by the amount of power converted by the frequency multiplier from frequency $f$ to frequency $2f$ to change the waveform shapes to continuous ones. The higher-order implementations can use harmonic components of order higher than two, or multiple harmonics. For operation at higher frequencies, the biharmonic Class-EM power amplifier can be energetically superior to a conventional Class-E power amplifier using the same power device and supplying the same output power at the same operating frequency. That is because it can tolerate slow transistor turn-off with much less efficiency loss. In addition, less input drive is needed for the biharmonic Class-EM power amplifier because slower switching times are tolerable when considering that switching times are inversely proportional to the square root of the input driving power.
Figure 7.50 shows the circuit schematic of a biharmonic Class-EM MOSFET power amplifier designed to operate at 3.5 MHz with second-harmonic power injection from an auxiliary amplifier operating at 7 MHz. The derivation of the ideal drain waveforms of the main amplifier assumes that the resultant current of the active device, operating as a switch, and its shunt capacitor contains only dc, fundamental, and second-harmonic components written as

\[
\begin{align*}
    i(\omega t) &= I_0 + I_{1A} \cos \omega t + I_{1B} \sin \omega t + I_{2A} \cos 2\omega t + I_{2B} \sin 2\omega t \\
&= I_0 + I_{1A} \cos \omega t + (I_{1B} + I_{2B}) \sin \omega t + I_{2A} \cos 2\omega t
\end{align*}
\]

(7.156)

where \( I_0 \) is the dc current, \( I_{1A} \) and \( I_{1B} \) are the quadrature fundamental current components and \( I_{2A} \) and \( I_{2B} \) are the quadrature second-harmonic current components, respectively. The shunt capacitances at the transistor drains can be composed of the device output capacitances and external capacitances.

For a 50% duty ratio when the switch is turned off during \( 0 < \omega t \leq \pi \), the current through the switch \( i(\omega t) = 0 \), and the current \( i_C(\omega t) \) flowing through the capacitor \( C \) fully represents the current \( i(\omega t) \) given in Eq. (7.156), reproducing the voltage across the switch by charging of this capacitor according to

\[
v(\omega t) = \frac{1}{\omega C} \int_0^{\pi} i(\omega t) \, d\omega t.
\]

(7.157)

The conditions for a biharmonic Class-Em optimum operation with jumpless voltage and current waveforms, \( v(\omega t) \) and \( i(\omega t) \), are written as

\[
i(\omega t) \bigg|_{\omega t = 0} = 0
\]

(7.158)
Substituting Eq. (7.156) into Eq. (7.157) and applying the boundary conditions given by Eqs. (7.158) through (7.161) yield

\[ I_{1A} = 0 \]  
\[ I_{1B} = -\frac{\pi}{2} I_0 \]  
\[ I_{2A} = -I_0 \]  
\[ I_{2B} = \frac{\pi}{4} I_0 . \]

As a result, the normalized steady-state idealized switch voltage waveform for a period of \( 0 \leq \omega t < \pi \) and current waveform for a period of \( \pi \leq \omega t < 2\pi \) are obtained by

\[
\frac{i(\omega t)}{I_0} = 1 - \frac{\pi}{2} \sin \omega t + \frac{\pi}{4} \sin 2\omega t - \cos 2\omega t \]  
\[
\frac{v(\omega t)}{V_{dd}} = \frac{2}{\pi} \left( 8\omega t + 4\pi \cos \omega t - \pi \cos 2\omega t - 4\sin 2\omega t - 3\pi \right)
\]

where \( V_{dd} \) is the dc supply voltage.

Figure 7.51(b) shows the normalized switch voltage and current waveforms for an idealized optimum biharmonic Class EM with second-harmonic power injection. From switch voltage and current waveforms, it follows that, when the transistor is turned on, there is no voltage across the switch and the current \( i(\omega t) \) consisting of the dc, fundamental, and injected second-harmonic components flows through the device. However, when the transistor is turned off, this current flows through the shunt capacitance \( C \). There is no jump in the switch current waveform at the instant of switching off compared to the switch current corresponding to a Class E with shunt capacitance, the voltage and current waveforms of which are shown in Fig. 7.51(a). However, the voltage peak factor is higher in a biharmonic Class-EM mode exceeding a value of 4. Note that injecting a higher-order harmonic component will generally increase the voltage peak factor even more. Also, there is no solution for a biharmonic Class-EM mode with third-harmonic injection and duty ratio of 50%. The voltage peak factor can exceed a value of 7 for a third-harmonic injection with a duty ratio of 33%. The voltage and current waveforms of the auxiliary amplifier are the usual waveforms corresponding to a Class E with shunt capacitance.
Fig. 7.51. Normalized ideal switch waveforms of (a) Class-E with shunt capacitance and (b) biharmonic Class-EM with second-harmonic power injection.

In a biharmonic Class-EM mode, it is assumed that the dc power \( P_0 = I_0 V_{dd} \) is equal to approximately 75% of the output load power \( P_{out} \) delivered to the load that results in

\[
I_0 V_{cc} = \frac{3}{4} \frac{P_{out}}{V_{dd}}. \tag{7.168}
\]

The fundamental-frequency load-network impedance of the main amplifier and the second-harmonic injection-port impedance of the auxiliary amplifier can be determined by a Fourier-series analysis of the voltage and current waveforms. As a result, the optimum shunt capacitance \( C \) and load-network impedance \( Z = R + jX \) for the main amplifier as a function of the dc supply voltage \( V_{dd} \) and output power \( P_{out} \) are written as

\[
C = \frac{3\pi}{64} \frac{P_{out}}{\omega V_{dd}^2}, \tag{7.169}
\]

\[
R = \frac{128}{9\pi^2} \frac{V_{dd}^2}{P_{out}}, \tag{7.170}
\]

\[
X = \frac{32\left(3\pi^2 - 32\right)}{9\pi^3} \frac{V_{dd}^2}{P_{out}}. \tag{7.171}
\]

whereas the optimum injection-port impedance \( Z_{inj} = R_{inj} + jX_{inj} \) for the auxiliary amplifier can be calculated from
\[ R_{\text{inj}} = \frac{128}{9(\pi^2 + 16)} \frac{V_{\text{dd}}^2}{P_{\text{out}}} \quad (7.172) \]
\[ X_{\text{inj}} = -\frac{16(3\pi^2 + 16)}{9\pi(\pi^2 + 16)} \frac{V_{\text{dd}}^2}{P_{\text{out}}} \quad (7.173) \]

The measured output power of a second-harmonic Class-\(E_M\) power amplifier was 13.2 W with overall \(PAE\) of 85.2\% at an operating frequency of 3.5 MHz. The injected power at \(2f\) necessary to achieve jumpless drain waveforms was measured as 29.8\% of the total dc power of the main amplifier instead of the theoretical value of 25\% due to the resistive power losses in reactive components, finite loaded quality factors of the series filters, and harmonic power conversions in the nonlinear device capacitances. To achieve simple and accurate design for the Class-\(E_M\) power amplifier with higher-order circuits, the numerical design procedure can be applied [67]. The analytical expressions for Class-\(E_M\) power amplifier considering the fundamental-frequency and harmonic components in the output currents of the main and auxiliary circuits are given in [68].

![Graph](image_url)

Fig. 7.52. Efficiency versus switching time for Class-\(E_M\) and Class-E power amplifiers.

Figure 7.52 shows the comparison between power-added efficiencies of the second-harmonic Class-\(E_M\) and classical Class-E power amplifiers as functions of the normalized transistor switching time \(\tau\) [66]. It is assumed that the switching time is inversely proportional to the input-drive power. The plots were simulated for power amplifiers delivering the output power 3.2 W at an operating frequency of 870 MHz using a pHEMT device with a gate periphery of 0.5 \(\mu\)m \(\times\) 50 mm in the main amplifier. The peak value of a \(PAE\) for the biharmonic Class-\(E_M\) power amplifier is 3.3\% lower than that for the classical Class-E power amplifier. However, a \(PAE\) for the Class-\(E_M\) power amplifier varies by just \(\pm2\%\) for all switching times from 6\% to 30\% of the period, whereas a \(PAE\) for the Class-E power amplifier drops monotonically from its peak to 73.5\% of its peak value for switching times of 30\% of the period. In an alternative
configuration of the biharmonic Class-EM power amplifier, one of the harmonics existing at drain of the main stage is filtered, amplified, phase shifted, and injected back to output of the main stage [69]. As a result, with second harmonic injection scheme delivering a 250-mW power while consuming 370 mW of power, an output power of 29 dBm with a power gain of 14 dB and a peak PAE of 63% was obtained at 2.4 GHz using a 0.25-μm pHEMT technology.

![Fig. 7.53. Circuit schematic of Class-EM power amplifier with isolation circuit.](image)

An analysis of the Class-EM power amplifier can be simplified and accurate explicit design equations for the load-network parameters can be derived by using an isolation circuit incorporated between the main and auxiliary circuits, thus resulting in a new configuration of the Class-EM power amplifier as shown in Fig. 7.53 [70]. Here, the main and auxiliary circuits each consists of a shunt capacitance ($C_{s1}, C_{s2}$), an RF choke ($L_{C1}, L_{C2}$), a series resonant circuit ($L_{1}C_{1}$ tuned at the fundamental $f_0$, $L_{2}C_{2}$ tuned to $2f_0$), and a series reactance ($X_1, X_2$), respectively. The isolation circuit consists of a series quarterwave transmission line ($TL_1$) and an open-circuit quarterwave stub ($TL_2$), providing a short-circuited termination at fundamental and odd harmonics with the corresponding open-circuited termination due to $TL_1$. Thus, the impedance $Z_M$ presented by the auxiliary circuit to the main circuit is sufficiently high with good isolation of the main circuit from auxiliary one at fundamental and odd harmonics. In this case, an analysis of the main and auxiliary circuits can be done separately.

**References**


