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High Gain Isolated Switched-Boost DC-DC Converter for PV Application

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Abstract—This paper presents a novel step-up DC-DC converter that combines a switched capacitor network with a boost converter. The proposed converter is well-suited for applications that require the delivery of high DC voltages to an AC inverter from a low DC voltage source such as Photovoltaic (PV). Using a low-turn-ratio transformer and a switched capacitor network, the converter can produce a high output voltage level while reducing voltage stress across the switches. The boost converter on the primary side also increases the input voltage, resulting in a higher power transfer from the input to the output. The proposed converter has an output voltage increase of ninefold when operated at a 30% duty cycle. The proposed topology was simulated using MATLAB/Simulink with an input voltage of 35 V, an output voltage of 320 V, and an output power of 315 W. The results showed that the converter has low switching and conduction losses, high voltage gain without excessive duty cycles and turns ratio, decreased voltage stress, and high efficiency.

Index Terms—Switched capacitor network, High voltage gain, PV system, Isolated DC-DC Converter

I. INTRODUCTION

There has been a significant increase in electrical energy demand due to the growth of the population and the expansion of various industries. The majority of energy consumed at present is derived from fossil fuels, which are responsible for global warming by emitting harmful gases. Developing an efficient, eco-friendly, and cost-effective green energy system such as PV, fuel cell, and wind is considered a key to solving the global power crisis. PV systems can provide a way forward for low-power applications because of their flexibility and controllability [1], [2], [11]. The PV generation has seen significant growth in recent years, with an expected annual growth rate of 18% between 2020 and 2024 [3], and is expected to become the most important source of renewable energy by 2040 [4]. A typical problem with PV production is that the PV panel output voltage is very small compared to the grid which is supposed to supply. Typically, a step-up DC-DC converter is employed as an intermediate power stage between PV panels and the grid to adjust the PV output voltage to a level acceptable for grid-connected applications [4], [11]. Recent research has introduced different DC-DC converters, including non-isolated and isolated configurations to achieve high voltage level [1]–[12]. Non-isolated topologies

require excessive circuit components and increased complexity to achieve high voltage level. Furthermore, the duty cycle must be high for a conventional boost converter to achieve a high output voltage, resulting in high conduction losses, high input current ripple, high switching losses, and low efficiency. Further, the lack of electrical isolation makes them unsuitable for applications requiring safety [12]. In accordance with the National Electrical Code, the solar PV system must be isolated from the AC grid for safety reasons since isolation from the AC grid enhances the lifetime of the PV panels by preventing potential-induced degradation (PID) [1]. Consequently, step-up isolated DC/DC converters for PV applications have gained considerable attention due to the safety benefits of isolation without additional bulky low-frequency line transformers. However, to achieve a high voltage gain with conventional isolated DC/DC converters, the turn ratio must be increased, which results in increased leakage inductance of the transformer and causes voltage stress across the semiconductors, leading to damage of the circuit components. There are many methods to obtain high voltage gain for isolated DC/DC converters such as voltage multiplier (VM) [1], [11], [13], switched capacitor (SC) [14]–[16], and Impedance source network (ZSN) [17], [18]. An isolated dc-dc converter using nondissipative snubber and SC method was proposed in [15]. To generate a large step-up gain, the capacitors on the secondary side are charged in parallel and discharged in series. The coupled inductor does not require a high turns ratio to achieve high step-up voltage gain by using the SC technique. However, the converter operates at a high duty cycle, increasing the conduction losses. In [19], the input voltage was increased using a boost converter on the primary side, and the voltage gain was enhanced by using flyback-forward on the secondary side.

This paper aims to propose a new high step-up isolated DC-DC converter by combining the advantages of switched capacitor cells proposed in [15] with the boost converter proposed in [19] and adding an extra diode in order to maximize the high voltage gain of switched capacitor cells and the high output voltage of boost converter. The turns ratio option can be spared at the expense of a switched capacitor network in order to achieve a very high voltage gain. The recommended DC-DC arrangement is characterized by low

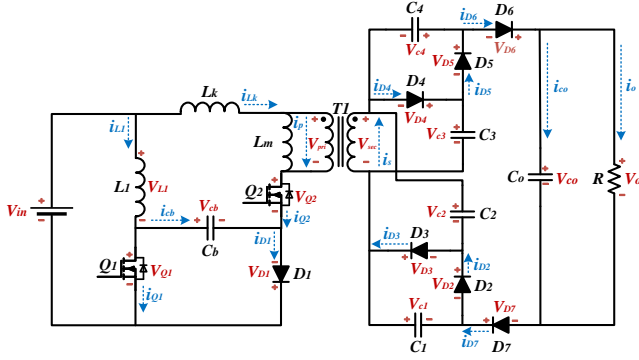


Fig. 1: The proposed converter.

switching and conduction losses, high voltage gain without excessive duty cycles, Low voltage stress, and high efficiency.

This article is organized as follows. The operation of the proposed converter in continuous conduction mode and its analysis are described in Section II. Section III provides a steady-state analysis of the proposed converter, which includes voltage gain and voltage stresses. Section IV presents a comparison of the proposed converter with several alternative typologies. The results of the simulation are presented in Section V. Finally, the conclusion is presented in Section VI.

II. OPERATING PRINCIPLES OF THE PROPOSED CONVERTER

The proposed converter is illustrated in Fig. 1. The primary side of the converter consists of one inductor (L_1), one diode (D_1), one capacitor (C_b), and two switches (Q_1, Q_2). In the secondary side of the transformer, there are five capacitors (C_1, C_2, C_3, C_4, C_o), and six diodes ($D_2, D_3, D_4, D_5, D_6, D_7$).

In order to simplify the circuit analysis of the proposed converter, the following assumptions are made:

- Passive components and switching devices are ideal.
- Capacitors ($C_1 - C_4, C_b$, and C_o) are large enough so that the voltages across them ($V_{c1} - V_{c4}, V_{cb}$, and V_o) are constant during the switching period.
- The transformer windings are perfectly coupled, which means the coupling coefficient is 1, and the leakage inductance can be ignored.
- Turns ratio of the transformer is $n = (n_{sec}) / (n_{pri})$

The major waveforms of the proposed converter are depicted in Fig. 2. Fig. 3 illustrates the four operating states of the proposed converter based on the on/off states of the MOSFETs (Q_1, Q_2) and the diodes ($D_1 - D_7$) during one switching cycle in CCM operation.

Mode I [$t_0 - t_1$]: As shown in Fig. 3a, switches (Q_1) and (Q_2) are turned-on and all diodes are turned off. Input voltage (V_{in}) charging inductor (L_1) via switch (Q_1). The boost capacitor (C_b) with the input voltage (V_{in}) charging the primary magnetizing inductance (L_m) through switch (Q_2).

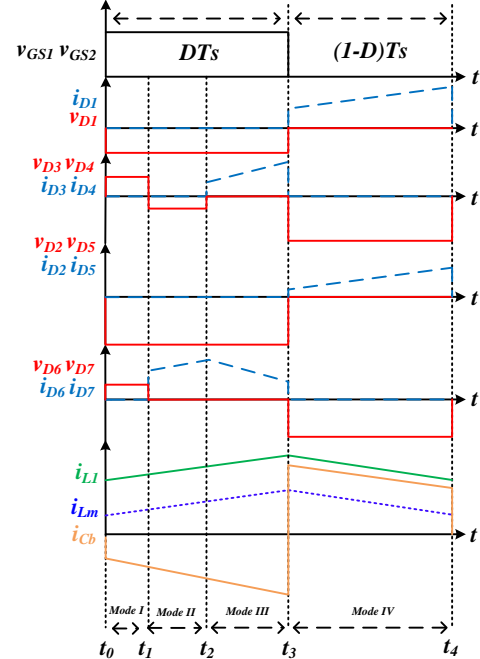


Fig. 2: Waveforms of the proposed converter.

The output capacitor (C_o) is releasing energy to the load (R). The current (i_{Lm}) increase linearly. When Diodes (D_6) and (D_7) are forward-biased, This mode ends.

Mode II [$t_1 - t_2$]: As shown in Fig. 3b switches (Q_1) and (Q_2) are still conducting. Diodes (D_6) and (D_7) are turned-on while diodes (D_1, D_2, D_3, D_4 , and D_5) are turned off. Input voltage (V_{in}) keeps charging inductor (L_1) via switch (Q_1), while the boost capacitor (C_b) with the input voltage (V_{in}) keeps charging the primary magnetizing inductance (L_m) through switch (Q_2). The primary magnetizing inductance (L_m) is connected to the secondary side, releasing energy to the output capacitor (C_o) and the load (R) via the series connection of (C_1) and (C_4). The primary magnetizing inductance keeps releasing energy, and the current (i_{Lm}) keeps increasing linearly. When diodes (D_4) and (D_5) are forward-biased, This mode ends.

Mode III [$t_2 - t_3$]: As shown in Fig. 3c switches (Q_1) and (Q_2) are still conducting. Diodes (D_3, D_4, D_6 , and D_7) are turned-on while diodes (D_1, D_2 , and D_5) are turned off. Input voltage (V_{in}) is still charging inductor (L_1) via switch (Q_1), and also the boost capacitor (C_b) with the input voltage (V_{in}) still charging the primary magnetizing inductance (L_m) through switch (Q_2). The primary magnetizing inductance (L_m) is connected to the secondary side, releasing energy to the output capacitor (C_o) and the load (R) via the series connection of (C_1) and (C_4) while charging (C_2) and (C_3) in parallel. The primary magnetizing inductance releases energy, and the current (i_{Lm}) still increases linearly. When switches (Q_1) and (Q_2) are turned off, and diode (D_1) is forward-

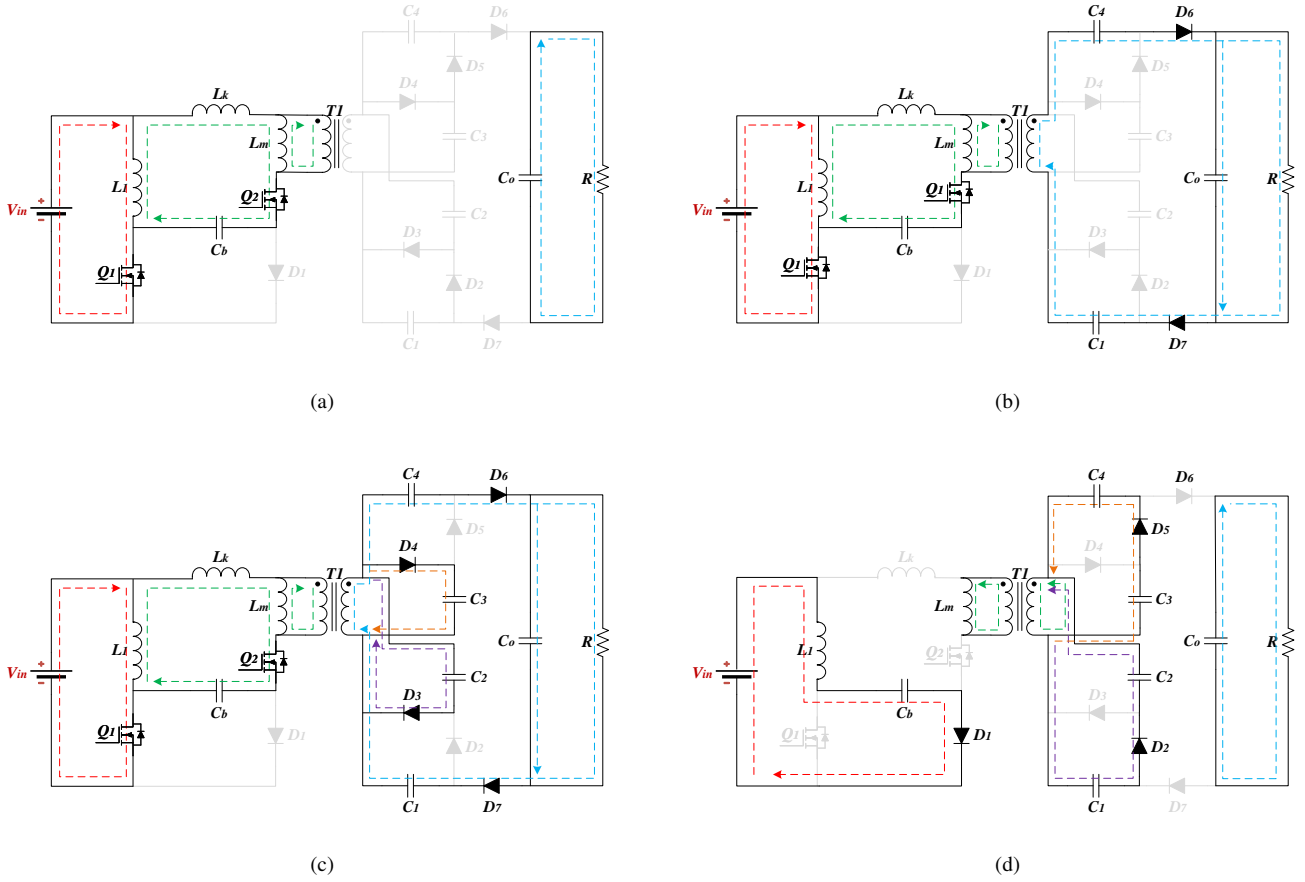


Fig. 3: Operation modes during ON/OFF switching at CCM. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV.

biased, This mode ends. The KVL equations for this mode are as follows:

$$V_{in} = V_{L1} \quad (1)$$

$$V_{Cb} + V_{pri} - V_{L1} = 0 \quad (2)$$

$$V_{pri} = \frac{V_{sec}^I}{n} \quad (3)$$

$$V_{sec}^I = (V_{Cb} + V_{in}) \times n \quad (4)$$

$$V_{sec}^I + V_{C4} - V_{Co} + V_{c1} = 0 \quad (5)$$

$$-V_{C2} + V_{sec}^I = 0 \quad (6)$$

$$-V_{C3} + V_{sec}^I = 0 \quad (7)$$

Mode IV [t_3-t_4]: As shown in Fig. 3d, switches (Q_1) and (Q_2) are turned-off. Diodes (D_1, D_2 , and D_5) are turned-on while diodes (D_3, D_4, D_6 , and D_7) are turned-off. The voltage (V_{in}) with inductor (L_1) charging the boost capacitor (C_b) through (D_1). The energy stored in the primary magnetizing inductance (L_m) supplies energy to the secondary side which is in series with capacitors (C_2) and (C_3) while charging (C_1) and (C_4) in parallel. The energy stored in the output capacitor (C_o) is released to the load (R). When the switches (Q_1) and (Q_2) are turned on and diode (D_1) is reverse-biased. This

mode ends. The KVL equations for this mode can be obtained as follows:

$$-V_{L1} - V_{Cb} + V_{in} = 0 \quad (8)$$

$$-V_{sec}^{II} - V_{c1} + V_{c2} = 0 \quad (9)$$

$$-V_{sec}^{II} + V_{c3} - V_{c4} = 0 \quad (10)$$

$$V_{Co} = V_o \quad (11)$$

III. MATHEMATICAL ANALYSIS OF THE PROPOSED CONVERTER

A. Voltage Gain

Using (6) and (7), the voltage across capacitors C_2 and C_3 can be represented as

$$V_{c2} = V_{sec}^I \quad (12)$$

$$V_{c3} = V_{sec}^I \quad (13)$$

With (12) and (13) substituted for (9) and (10), the voltage across C_1 and C_4 can be expressed as

$$V_{c1} = V_{sec}^I - V_{sec}^{II} \quad (14)$$

$$V_{c4} = V_{sec}^I - V_{sec}^{II} \quad (15)$$

TABLE I: Performance Comparison of the Proposed

Topology	Number of Components					Voltage Gain (G)	Voltage Gain Range (D): 0 → 0.9 at n = 1	I/O Voltage (f _S), (P _O)	Turn Ratio (n)	Duty Cycle (D)	Efficiency (η)
	L	C	S	D	MC						
[9]	2	5	1	7	1	$G = \frac{n(1+D)}{(1-D)^2}$	$G = 1 \rightarrow 190$	12 V/200 V 100 kHz 100 W	1:2	0.57	85%
[10]	0	6	4	4	2	$G = \frac{4n}{(1-D)}$	$G = 4 \rightarrow 40$	36 V/380 V 50kHz 1 KW	1:1.2	0.54	90.3%
[11]	1	4	2	5	1	$G = \frac{n(2-D)}{(1-D)^2}$	$G = 2 \rightarrow 110$	40 V/380 V 50 kHz 500 W	1:1.9	0.50	90.67%
[15]	1	7	1	6	1	$G = \frac{n(2+D)}{(1-D)}$	$G = 2 \rightarrow 29$	24 V/400 V 50 kHz 200 W	1:2	0.68	93.4%
[19]	1	4	3	3	1	$G = \frac{n(2-D)}{(1-D)^2}$	$G = 2 \rightarrow 110$	48 V/400 V 50 kHz 800 W	1:2	0.45	93.6%
Proposed	1	6	2	7	1	$G = \frac{n(6-5D+D^2)}{(1-D)^2}$	$G = 6 \rightarrow 231$	35 V/ 320 V 50 kHz 315 W	1:1	0.30	91.6%

Note : L: inductor, C: Capacitor (including input and output capacitors), S: Switch, D: Diode, MC: Magnetic coupling (including transformer and coupled inductors).

The voltage across the secondary winding of the transformer can be calculated by substituting (14) and (15) into (5)

$$V_o = 3V_{sec}^I - 2V_{sec}^{II} \quad (16)$$

$$V_{sec}^{II} = \frac{3V_{sec}^I - V_o}{2} \quad (17)$$

The following equation is derived by utilising the volt-second balancing principle

$$\int_0^{DT_s} V_{sec}^I dt + \int_{DT_s}^{T_s} V_{sec}^{II} dt = 0 \quad (18)$$

Substituting (17) into (18) yields the following equations

$$V_{sec}^I \times DT_s + \frac{3V_{sec}^I - V_o}{2} \times (1-D)T_s = 0 \quad (19)$$

$$V_{sec}^I(3-D) = V_o(1-D) \quad (20)$$

In order to determine the voltage of the boost capacitor, the following equation can be used

$$V_{cb} = \frac{1}{(1-D)} \quad (21)$$

Substituting (4) and (21) into (20), the voltage gain is

$$G = \frac{V_o}{V_{in}} = \frac{n(6-5D+D^2)}{(1-D)^2} \quad (22)$$

B. Voltage stress

The voltage stress of the proposed converter for switches (Q_1) and (Q_2) are: Voltage stress across switch (Q_1) is

$$V_{Q1} = \frac{V_{in}}{(1-D)} \quad (23)$$

Voltage stress across switch (Q_2) is

$$V_{Q2} = \frac{V_{in}}{(1-D)^2} \quad (24)$$

IV. COMPARISON OF THE PROPOSED CONVERTER

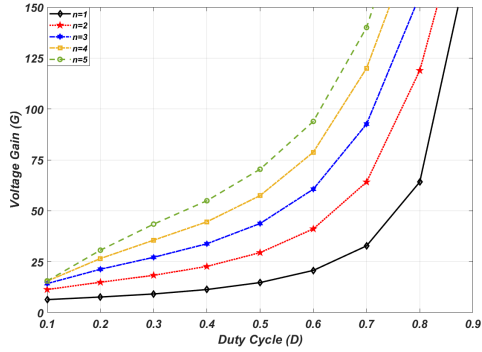
A number of comparisons are made in this section in order to demonstrate the superiority of the proposed converter. Comparisons are made in terms of voltage gain, efficiency, and output power. As the turn ratio increases, the leakage inductance increases, resulting in voltage stress across the switches. Fig. 4a shows that the converter voltage gain increases with increasing transformer turn ratio. Voltage gain is dependent on both the switched capacitor cells and the transformer's turns ratio. Traditionally this causes a problem with the voltage stress across the switches. However, the voltage stress is in the proposed topology reduced because it is compensated by the secondary switched capacitor cells and the boost converter.

At 315 W output power, 320 V output voltage, and 0.3 duty cycle, the efficiency of the proposed converter was measured.

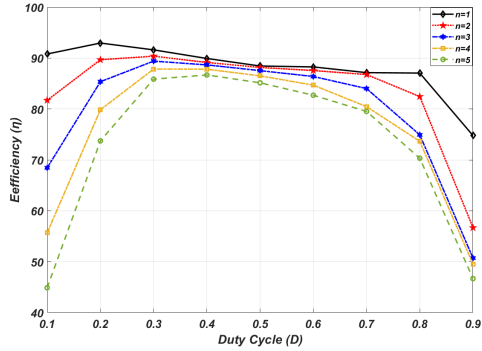
$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times i_{out}}{V_{in} \times i_{in}} \times 100\% = 91.6\% \quad (25)$$

Fig. 4b. illustrates the relationship between efficiency and the duty cycle. It is evident from the comparison that efficiency increases while the turn ratio decreases simultaneously. Switched capacitor extensions contribute a substantial amount to voltage step-up operations, which are praised for their higher efficiency at lower duty ratios and turn ratios. The results also show that higher efficiency is achievable only from 10% to 40% at a turns ratio of 1. The comparison between output power, efficiency, and voltage gain is shown in Fig. 4c. When the output power increases, efficiency is increased while voltage gain is decreased.

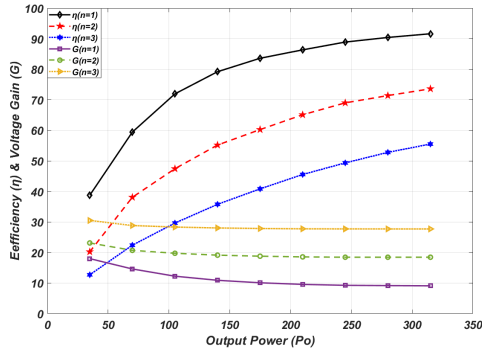
Table. I compares the proposed converter with the converter in [9]–[11], [15], [19] in terms of the number of components, voltage gain, input and output voltages, switching frequency, power rating, duty cycle, and efficiency. There is no doubt that the proposed converter contains the largest component. However, as shown in Fig. 4d, it has the highest voltage gain



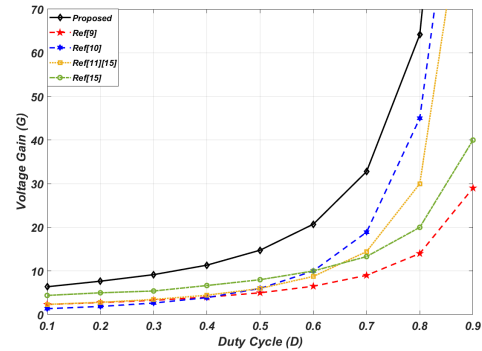
(a)



(b)



(c)



(d)

Fig. 4: (a) Voltage Gain vs Duty Cycle of the Proposed Converter, (b) Efficiency vs Duty Cycle of the Proposed Converter, (c) Output Power vs Voltage Gain & Efficiency of the Proposed Converter, and (d) Voltage Gain vs Duty Cycle at Turn Ratio $n=1$ Comparing with Different Converters.

TABLE II: Components Parameters

Components	Parameters	
Input voltage	V_{in}	35 V
Duty cycle	D	0.30
Capacitors	$C_{1,2,3,4}$	50 μf
	C4AEGBW5500A3LJ	
	$C_{b,o}$	100 μf
Inductor	R60EW61005000K	
	L_1	150 μH
Switching frequency	74437529203151	
	f_s	50 kHz
MOSFETs	$Q_{1,2}$	1200 V, 44 A
	NVH4L040N120M3S	
Diodes	D_{1-7}	1000 V, 80 A
	RURG80100	
Magnetizing inductance	L_m	250 μH
Leakage inductance	L_k	0.4 μH
Turn ratio	n	1:1

at a turn ratio of 1 and operates at a low duty cycle. As a result, condition losses and voltage stress are reduced.

V. RESULT AND SIMULATION

The proposed topology is simulated and tested using MATLAB/Simulink. Table. II shows the parameters of the proposed converter's components.

Fig. 5 shows the simulation waveforms of the proposed converter according to the parameters and conditions are shown in Table. II. The input voltage (V_{in}) is shown in Fig. 5a, while the output voltage (V_o) is depicted in Fig. 5b. Fig. 5c and Fig. 5d show the waveforms of the voltage across the primary and the secondary of the transformer (V_{pri} , V_{sec}). The current through the inductor (i_{L1}) is shown in Fig. 5e. The output current (i_{OUT}) can be seen in Fig. 5f. The voltage stress across switches (Q_1 , Q_2) are presented in Fig. 5g and Fig. 5h. The voltage across capacitors (C_1 , C_2 , C_3 , C_4) illustrates in Fig. 5i, j, k, and l. The output voltage is boosted from an input of 35 V and delivered to the transformer at a low-duty cycle and turn ratio.

VI. CONCLUSION

A new high step-up isolated DC-DC converter is presented in this paper that not only reduces switching losses and stress on the switches but also increases voltage gain at a reduced duty ratio. Using a switched capacitor cells on the secondary side and a boost converter on the primary side results in a high voltage gain without increasing the voltage stress on the switches and the turn ratio of the transformer. The proposed converter provides several features: a low input current, low voltage stress across semiconductors, and low-power rating components. Comparative studies are conducted to highlight the isolated DC-DC converter's advantages and demonstrate its capability to provide practical configurations. The proposed topology is simulated using MATLAB/Simulink to verify the converter's performance. The proposed converter was capable of boosting 35V to 320V. The efficiency of the proposed converter is approximately 91.6% at the rated output power.

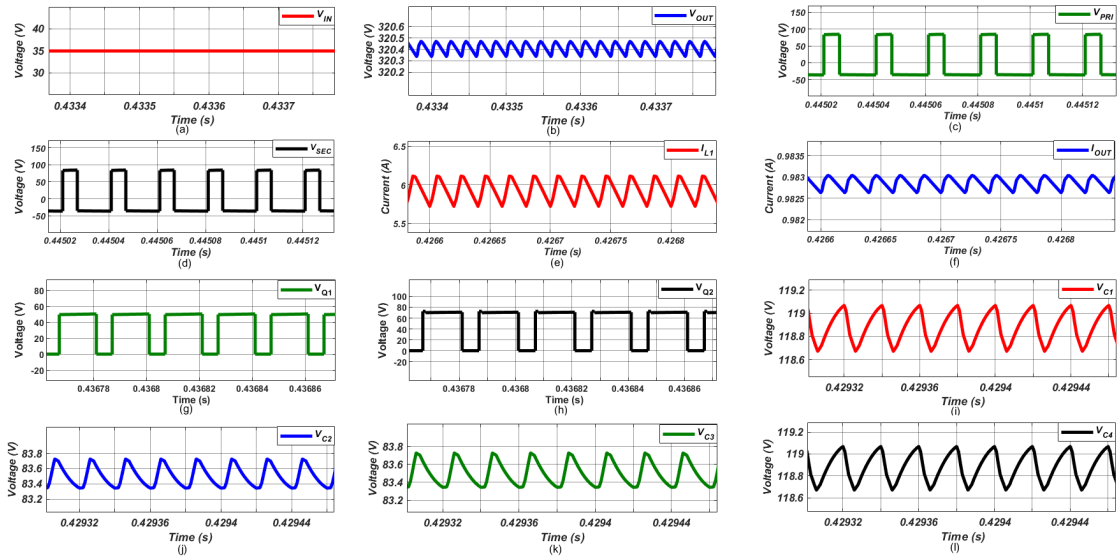


Fig. 5: (a) The input voltage (V_{in}), (b) The output voltage (V_o), (c) The voltage across the primary of the transformer (V_{pri}), (d) The voltage across the secondary of the transformer (V_{sec}), (e) The current of the inductor (i_{L1}), (f) The output current (i_{OUT}), (g) Voltage across switch (Q_1), (h) Voltage across switch (Q_2), (i) Voltage across capacitor (V_{C1}), Voltage across capacitor (V_{C2}), Voltage across capacitor (V_{C3}), and (e) Voltage across capacitor (V_{C4}).

VII. ACKNOWLEDGMENT

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