Single-Phase Virtual-Ground Transformerless Buck-Boost Inverters

Fazal Akbar, Ahmad Elkhateb, Senior Member IEEE, Hafiz Furqan Ahmed, Ashraf Ali Khan, Member IEEE, Honnyong Cha, Senior Member, IEEE, and Jung-Wook Park, Senior Member, IEEE.

Abstract—This paper presents a new family of transformerless buck-boost voltage-source inverter topologies for photovoltaic systems. Due to variations in irradiance, temperature, and shading effects, the terminal voltages of photovoltaic panels can vary, making the use of buck-boost inverters crucial. The proposed topologies have a virtual-ground feature which effectively mitigates the common-mode voltage issue and results in low leakage current. The simple inductor-based proposed inverter can achieve a wide gain range. Also, other counterparts obtained by extending the underlying concept of the simple inductor-based proposed inverter, such as the switched inductor, three-winding coupled inductor, and series capacitor converters, are capable of achieving high boost voltage gain with lower duty ratios. Comprehensive circuit analyses are provided, along with simulation results, to confirm the operation of each proposed topology. Additionally, experiment findings for a 500 W prototype built on the simple inductor topology are presented to support the theoretical analysis and effectiveness of the proposed designs.

I. INTRODUCTION

Photovoltaic (PV) panels have become increasingly popular as a source of clean energy. However, their terminal voltages are often variable, making it necessary to use isolated or non-isolated buck-boost inverters (BBIs) to connect them to the grid or load. Transformerless BBIs are more commonly used due to their low cost, high efficiency and compact size. However, because transformerless inverters lack galvanic isolation, they must address the issue of ground leakage current, which is caused by parasitic capacitances ($C_{pv1}$ and $C_{pv2}$) of the PV panel due to the high-frequency common-mode voltage ($V_{cm}$) fluctuations, as presented in Fig. 1. To avoid negative impacts from the leakage current, the leakage current should not exceed 300 mA [1].

Well-known examples of transformerless topologies include full-bridge voltage-source inverters and current-source inverters. However, voltage-source inverters can only step down the input voltage, while current-source inverters can only step it up. A typical approach for achieving step up/down function is to cascade a conventional boost converter [2], [3] to a voltage source inverter or a buck converter with a current source inverter. This two-stage inverter is effective but reduces overall efficiency due to the high-frequency switching stages. Several single-stage inverters, such as impedance-source inverters, integrated inverters, and combined inverters, have been developed to reduce power processing stages. Impedance-source inverters [4] overcome the limitations of voltage-source inverters and current-source inverters, but the passive components decrease power density. Moreover, simultaneous switching and voltage spikes across all switches degrade system efficiency [5].

Another block diagram of grid-tied inverter

![Fig. 1. Generic block diagram of grid-tied inverter](image1)

Fig. 2. Configurations of inverters with AVG circuit (a) Type I (b) Type II.
Another promising category for dc-ac conversion is combined inverter topologies. Combined inverters are originated from the combination of different inverters like a buck, boost, and buck-boost converters. In [16], a doubly grounded transformerless inverter is developed by combining buck and buck-boost converters. This inverter has no current shoot-through and leakage current problem, but it can perform only the step-down function. The inverter in [17] can perform the buck-boost function and is developed from the combination of two buck-boost converters. It clamps the common mode voltage, but its input current is pulsating and requires more passive components. Differential-boost Inverter (DBI) consists of two bidirectional boost converters [18] and can perform the buck-boost function with low common-mode voltage, which is a vital property for PV applications. However, all the switching devices of DBI [18] work at high or medium frequency, and in consequence, the switching loss is high. Furthermore, the core and copper loss are increased because of the circulating current in the step-up inductors. Yu Tang et al. used a half-cycle modulation strategy to address these issues and proposed an improved DBI [19]. This inverter can achieve high efficiency because only two switches operate simultaneously at a high frequency, and there is no circulating current through the inductors. In spite of improvements, the combined inverters have a downside of employing several inductors. To decrease the size of magnetics, Manitoba BBI [20] and virtual-ground BBI [21] are recently proposed. Manitoba inverter needs only two inductors used for buck-boost operations and removing the high-frequency component of the grid current. Moreover, it resolves the common-mode voltage problem by employing the active-virtual-ground (AVG) concept [22]-[24]. The typical configurations of inverters with AVG circuit are presented in Fig. 2. The two terminals of the AVG circuit are connected to the line and neutral of the grid, while the third terminal is connected to either the positive or negative terminal of the dc-link as displayed in Figs. 2(a) and 2(b) respectively. The bidirectional switching devices ($S^+$ and $S^-$) in the AVG circuit operate alternatively at line frequency during the AVG capacitor $C_{AVG}$ clamps the voltage between the grid and dc bus to mitigate the issue of the common-mode voltage. Moreover, the circuit is given the name AVG because of the impedance of voltage sources and the capacitor $C_{AVG}$ are negligible at high-frequency signals point of view, and the dc-link always seems connecting to the network ground. The downside of Manitoba BBI is that it needs eight power switches. Both inductors still need to be designed with saturation current equal to the summation of input and output current. In contrast, virtual-ground BBI [21] has low common-mode voltage and needs two inductors in which one is dedicated for buck-boost operation while the other is dedicated for filtering the output grid current only. However, it is unidirectional and requires seven semiconductor devices and two output filter capacitors.

It is noteworthy that all the above-mentioned buck-boost inverters [3]-[21] have practically limited voltage step-up gain due to the parasitic resistances of the components at a high duty ratio. Various research efforts are therefore dedicated to developing power inverters with high voltage gain capabilities in [25]-[27]. However, these topologies suffer from the severe ground leakage current problem. Switched-capacitor inverters [28], [29] and differential Y-source inverters [30] have low ground leakage current with high voltage step-up capabilities. Still, many active and passive components are the downside of these topologies.

This article proposes new topologies of single-phase transformerless BBI for PV systems to overcome the aforementioned challenges. The general configuration of the proposed inverters consists of a boost cell, input capacitor $C_{in}$, output capacitor $C_d$, and four line-frequency switches $S_1$-$S_4$ as presented in Fig. 3(a). Type I inverter, which is presented in Fig. 3(b) uses a simple inductor structure, while types II, III, and IV inverters, as presented in Figs. 3(c) to 3(d) use switched-inductor [31], three-winding coupled inductor [30], and series-capacitor high conversion ratio [32] structures in place of boost...
cell, respectively. The working principle of all the proposed inverters is similar; that is, the step-up cell is responsible for generating a rectified sinusoidal voltage with dc-offset equivalent to the input voltage across the capacitor \( C_o \), which is later on removed with the help of line frequency switches to obtain pure sinusoidal voltage. Type I Inverter needs one inductor only to provide a wide range of buck-boost operation, while the other three types can achieve high boost gain at small duty ratios. The proposed inverters also have low common-mode voltage and leakage current due to virtual-ground characteristics and can achieve high power conversion efficiency because there are only two high-frequency (HF) switches in Type I, II, and III inverters while four HF switches in Type IV Inverter. The line-frequency (LF) switches have low voltage and current stresses which further allow selecting MOSFETs with low drain-source on resistances irrespective of taking in consideration their switching losses. The HF switches in this paper refer to the switching devices that operate at the switching frequency which is 50 kHz, while the LF switches are the switching devices that operate at 50 Hz.

![Block diagram of gate signals generation of the proposed type I inverter.](image)

**Fig. 4.** (a) Block diagram of gate signals generation of the proposed type I inverter. (b) Gate signals and operational modes.

This paper is organized as follows: Section II describes the modulation strategy and operating modes of the proposed Type I Inverter, followed by its leakage current consideration and design guidelines in section III, and its experiment verification in section IV. Finally, the switching strategies, design guidelines, and simulation results of the proposed extended high-gain topologies (types II, III, and IV) are included in section V, while the concluding remarks are provided in section VI.

II. MODULATION STRATEGY AND CIRCUIT OPERATION OF THE PROPOSED TYPE I INVERTER

In proposed inverters (Type I to Type IV), the switching devices \( S_a \) and \( S_d \) are ON for only the positive half of the output voltage, while the switching devices \( S_b \) and \( S_c \) are ON for only negative half of the output voltage. The output voltage \( v_o \) can thus be represented by the following equation.

\[
v_o = v_o \sin \omega t = \begin{cases} 
  v_C - v_{in}, & \text{for } v_o > 0 \\
  v_{in} - v_C, & \text{for } v_o < 0
\end{cases}
\]

Where \( v_C \) is the peak value of output voltage, \( v_C \) is the voltage of capacitor \( C_o \), and \( v_{in} \) is the input voltage. From (1), the voltage on capacitor \( v_C \) can be written as

\[
v_C = v_{in} + |v_o| = v_{in} + |v_o \sin \omega t|.
\]

In order to generate \( v_C \) from the proposed Type I inverter, the complementary switches \( S_i \) and \( S_j \) are operated at HF through a proper modulation scheme such that

\[
v_C = v_{in} + |v_o \sin \omega t| = \frac{v_{in}}{1 - d_1}.
\]

Where \( d_1 \) is the duty ratio of the switching device 1. Rearranging (3), \( d_1 \) is calculated as follows

\[
d_1 = \frac{|v_o \sin \omega t|}{v_{in} + |v_o \sin \omega t|}.
\]

The duty ratio \( d_1 \) can be written in respect of the voltage gain \( G = \frac{v_o}{v_{in}} \) as presented in (5)

\[
d_1 = \frac{|G \sin \omega t|}{1 + |G \sin \omega t|}.
\]

Fig. 4(a) depicts the block diagram for generating the proposed Type I inverter’s gate signals. It can be observed that the gate signals for the switching device \( S_1 \) is acquired from (5), which indicates that the reference \( v_{ref} = G \sin \omega t \) is created. Then its absolute value \( (|G \sin \omega t|) \) is divided by \((1 + |G \sin \omega t|) \). The quotient is then compared with the triangular carrier \( v_{tri} \) to obtain gate signals for \( S_1 \). The complementary signals of \( S_1 \) are then applied to \( S_2 \). The gate signals and operational modes of the proposed Type I inverter in the complete line cycle of the output voltage are presented in Fig. 4(b). Modes 1 and 2 appear for \( v_o > 0 \), while modes 3 and 4 occur for \( v_o < 0 \). The current paths during each mode of operation are presented in Fig. 5.

1) **Mode-1:** In this mode, the switching devices \( S_1, S_b \) and \( S_c \) are ON. The inductor \( L \) stores energy while the capacitor \( C_o \) supplies energy to the load. The current paths are presented in Fig. 5(a) and the inductor current ripple \( \Delta i_L \) is given by

\[
\Delta i_L = \frac{v_o d_1 T_s}{L}.
\]

Where \( T_s \) is the switching time period.

2) **Mode-2:** In this mode, the switching devices \( S_2, S_a \) and \( S_d \) are ON. The inductor \( L \) provides energy to both capacitor \( C_o \) and the load. The current directions are presented in Fig. 5(b) while \( \Delta i_L \) is given by

\[
\Delta i_L = -\frac{v_o (1 - d_1) T_s}{L}.
\]

3) **Mode-3:** In this mode, the switching devices \( S_1, S_b \) and \( S_c \) are ON. The inductor \( L \) stores energy, and the output capacitor \( C_o \) delivers energy to the load. The current directions are presented in Fig. 5(c) and \( \Delta i_L \) is similar to mode 1.

4) **Mode-4:** In this mode, the switching devices \( S_2, S_b \) and \( S_d \) are ON. The inductor \( L \) provides energy to both the output capacitor \( C_o \) and the load. The current directions are presented in Fig. 5(d) while \( \Delta i_L \) is given by

\[
\Delta i_L = \frac{v_o (1 - d_1) T_s}{L}.
\]
produce small leakage currents. On the other hand, the leakage current becomes zero if there are no variations across the parasitic capacitances' voltages.

The typical grid-connected configuration of the proposed Type I inverter is presented in Fig. 6. The parasitic capacitances of PV panel are denoted by \(C_{p1}\) and \(C_{p2}\) while their voltages are represented by \(v_{p1}\) and \(v_{p2}\). The inductor \(L_o\) filters the high-frequency harmonics and is also required for conventional grid-tied inverters. Voltages across the parasitic capacitances in positive and negative half-cycles of output voltage can be obtained from the simplified circuits presented in Figs. 7(a) and (b). The simplified circuits are obtained by replacing always on and off switches with short-circuit and open-circuit respectively. Voltages appearing across the parasitic capacitances are included in Table I. Throughout the output voltage's positive-half-cycle, the leakage current is zero because the ac ground is directly connected to the dc bus and the parasitic capacitance's voltages \(\left(v_{p1}, v_{p2}\right)\) are constant. On the other hand, \(v_{p1}\) and \(v_{p2}\) change according to both capacitor voltage \(v_C\) and input voltage in the negative half-cycle. Input voltage is constant and according to (3), \(v_C\) varies sinusoidally with line frequency. This implies that there is no substantial high-frequency variations across the parasitic capacitances and the leakage current will be low. From the standpoint of high-frequency signals, the capacitor \(C_o\) offers a low-impedance route that virtually links the ground of the grid to the common-terminal of the photovoltaic panel making the virtual grounded circuit.

### Voltage Gain

The maximum duty ratio \(D_{1,max}\) of switch \(S_1\) can be obtained from (4) and is given by

\[
D_{1,max} = \frac{V_o}{V_{in} + V_o}.
\]
Using (9), the voltage gain $G$ can be expressed in terms of $D_{1,\text{max}}$ as in (10):

$$G = \frac{V_o}{V_{in}} = \frac{1 - D_{1,\text{max}}}{D_{1,\text{max}}}.$$  \hspace{1cm} (10)

The graph of $G$ versus $D_{1,\text{max}}$ is presented in Fig. 8. The proposed Type I inverter will perform buck function if $D_{1,\text{max}} < 0.5$ and boost function if $D_{1,\text{max}} > 0.5$.

C. Switch Selection

The voltage and current ratings are used to choose the switching devices. The maximum drain-to-source voltages appearing across the proposed Type I inverter's switches are given by

$$V_{ds-1} = V_{ds-2} = V_{in} + V_o,$$  \hspace{1cm} (11)
$$V_{ds-a} = V_{ds-b} = V_{ds-c} = V_{ds-d} = V_o.$$  \hspace{1cm} (12)

Where $(V_{ds-1}, V_{ds-2})$ and $(V_{ds-a} - V_{ds-d})$ represent the maximum drain-to-source voltages of the switching devices $(S_1, S_2)$ and $(S_a - S_d)$ respectively. The voltage stresses of the switching devices can be normalized to the peak output voltage $V_o$ and represented in terms of voltage gain $G$ as follows

$$\frac{V_{ds-1}}{V_o} = \frac{V_{ds-2}}{V_o} = \frac{1 + G}{G},$$  \hspace{1cm} (13)
$$\frac{V_{ds-a}}{V_o} = \frac{V_{ds-b}}{V_o} = \frac{V_{ds-c}}{V_o} = \frac{V_{ds-d}}{V_o} = 1.$$  \hspace{1cm} (14)

Similarly, the maximum current and rms current flowing through the switching devices are normalized to the output current's maximum value $I_o$ and are calculated as presented below in (15)-(19):

$$\frac{I_{S1\text{rms}}}{I_o} = \frac{1}{\pi} \int_0^\pi [G\sin^2\omega t(1 + G\sin\omega t)]d(\omega t).$$  \hspace{1cm} (15)
$$\frac{I_{S2\text{rms}}}{I_o} = \frac{1}{\pi} \int_0^\pi [\sin^2\omega t(1 + G\sin\omega t)]d(\omega t).$$  \hspace{1cm} (16)

$$\frac{I_{S\text{rms}}}{I_o} = \frac{1}{2\pi} \int_0^{\pi} \sin^2\omega t d(\omega t).$$  \hspace{1cm} (17)

Where $(I_{S1\text{rms}}, I_{S2\text{rms}})$ and $(I_{Sa} - I_{Sd})$ represent the rms current while $(I_{S1}, I_{S2})$ and $(I_{Sa} - I_{Sd})$ represent the maximum current flowing through the switching devices $(S_1, S_2)$ and $(S_a - S_d)$ respectively.

D. Input Capacitor Selection

Similar to conventional inverters, the proposed Type I inverter also requires an input capacitor for power decoupling. The value of the input capacitor can be calculated as follows

$$C_{in} = \frac{P_{in}}{2\pi f_o V_{in} \Delta V_{in}}.$$  \hspace{1cm} (20)
A common output voltage \( V_1 \geq V_0 = V \), \( I_1 \) is the output current and \( I_0 \) is the inductor current. Putting these values in (21) for the maximum voltage gain \( G \), the increase in capacitance is maximum at this point.

E. Inductor Design

The maximum inductor current ripple \( \Delta i_{L_{\text{max}}} \) calculated from (6), (9) and (10) is given by

\[
\Delta i_{L_{\text{max}}} = \frac{V_{\text{in}} T_s G}{L (1 + G)}. \tag{21}
\]

Where \( \Delta i_{L_{\text{max}}} = y I_L \), \( y = 10\% \) to \( 50\% \), and the maximum inductor current \( I_L = (1 + G) I_o \). Putting these values in (21), the formula for inductance \( L \) is calculated as follows

\[
L = \frac{V_{\text{in}} T_s G}{y(1 + G)^2 I_o} = \frac{V_o T_s}{y(1 + G)^2 I_o}. \tag{22}
\]

Replacing \( V_s T_s / y I_o \) in (22) by constant \( k_1 \), the normalized inductance \( L / k_1 \) is plotted in Fig. 10. The graph implies that the value of inductance \( L \) should be chosen at the minimum voltage gain \( G \) because the inductance is maximum at this point.

F. Filter Capacitor Selection

The function of the filter capacitor \( C_o \) is to limit the output voltage ripple and the leakage current. The general formula for calculating the value of the filter capacitor is given by

\[
C_o = \frac{i_c \Delta t}{\Delta v} \tag{23}
\]

Where \( i_c \) is the current flowing through the capacitor during \( \Delta t \), and \( \Delta v \) is the voltage ripple of the output or capacitor voltage. \( \Delta v = z V_o \) and \( z \) is typically selected in the range of \( 5\% \) to \( 10\% \). As explained in mode analysis, the output current \( i_o \) flows through the capacitor \( C_o \) for duty ratio \( d_1 \). This implies that the required value of capacitance can be calculated from (23) using the maximum duty ratio and is given by

\[
C_o \geq \frac{i_o D_{1_{\text{max}}} T_s}{z V_o} = \frac{I_o G T_s}{z V_o (1 + G)}. \tag{24}
\]

Replacing \( I_s T_s / z V_o \) in (24) by constant \( k_2 \), the normalized capacitance \( C_o / k_2 \) is drawn in Fig. 11. The diagram implies that the value of the capacitance \( C_o \) should be selected at maximum voltage gain because the required capacitance increases with the voltage gain \( G \). The increase in capacitance is actually due to an increase in the voltage ripple as well as the increase in the voltage gain.

<table>
<thead>
<tr>
<th>Table II. Electrical Specifications</th>
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<tbody>
<tr>
<td>Output power</td>
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<tr>
<td>Input voltage ( V_{\text{in}} )</td>
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<tr>
<td>Output voltage ( V_{\text{out}} )</td>
</tr>
<tr>
<td>Switching frequency</td>
</tr>
<tr>
<td>Switches ( (S_s, S_e) )</td>
</tr>
<tr>
<td>Switches ( (S_1, S_2, S_3, S_6) )</td>
</tr>
<tr>
<td>Inductor ( L )</td>
</tr>
<tr>
<td>Capacitor ( C )</td>
</tr>
<tr>
<td>Parasitic capacitances ( C_{p1}, C_{p2} )</td>
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</table>

IV. EXPERIMENT RESULTS

To verify the performance of the proposed Type I inverter, experiments are conducted in both the step-down and the step-up modes of operation. The electrical specifications for the experiment setup are included in Table II and the hardware
Fig. 14. Experiment waveforms in the step-up mode. (a) Voltage across the filter capacitor $v_C$ and drain-source voltages of switches $S_1$ and $S_2$. (b) Drain-source voltages of switches $S_a$, $S_b$, $S_c$ and $S_d$.

Fig. 15. Voltages across the parasitic capacitances $v_{p1}$, $v_{p2}$ and their leakage currents $i_{{LKG1}}, i_{{LKG2}}$ in the step-up mode.

Fig. 16. Experiment waveforms in the step-down mode. (a) $V_{in}$, $v_C$, $i_L$ and $i_o$. (b) Voltage $v_C$ and drain-source voltages of switches $S_1$ and $S_2$.

Prototype picture is shown in Fig. 12. Figs. 13 to 15 show the waveforms in the step-up mode with a 100 V input voltage.

Gate signals for the switching devices $(S_1, S_2)$ and $(S_a - S_d)$ are presented in Fig. 13(a) while the input voltage $V_{in}$, output voltage $v_o$, output current $i_o$ and inductor current $i_L$ are presented in Fig. 13(b). The voltage across the capacitor $v_C$ and drain-source voltages of HF switches $v_{ds-1}$, $v_{ds-2}$ are presented in Fig. 14(a). The drain-source voltages of LF switches $v_{ds-a}$, $v_{ds-d}$ are presented in Fig. 14(b). Waveforms of voltages across the parasitic capacitances and the corresponding leakage currents are presented in Fig. 15.

Similarly, Figs. 16 and 17 display the experiment results in the step-down mode with an input voltage of 200 V. Input voltage, output voltage, output current and inductor current are presented in Fig. 16(a), while the voltage across the capacitor $v_C$ and drain-source voltages of HF switches are presented in Fig. 16(b). The drain-source voltages of LF switches are similar to those of the step-up mode, thus, they are not presented again. Voltages across the parasitic capacitances and the leakage currents are presented in Fig. 17.

Fig. 17. Voltages across the parasitic capacitances $v_{p1}$, $v_{p2}$ and their leakage currents $i_{{LKG1}}, i_{{LKG2}}$ in the step-down mode.

Fig. 18. (a) Efficiency and THD versus input voltage. (b) Efficiency versus power at different input voltages.
Table III. Comparison of the proposed type I and conventional buck-boost inverters.

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<tbody>
<tr>
<td>Voltage gain (G)</td>
<td>( \frac{D}{1-D} )</td>
<td>( \frac{D}{1-D} )</td>
<td>( \frac{D}{1-D} )</td>
<td>( \frac{D}{1-D} )</td>
<td>( \frac{D}{1-D} )</td>
<td>( \frac{D}{1-D} )</td>
<td>( \frac{D}{1-D} )</td>
</tr>
<tr>
<td>Switches</td>
<td>( 6 (S_1 - S_6) )</td>
<td>( 4 (S_1 - S_4) )</td>
<td>( 4 (S_1 - S_4) )</td>
<td>( 6 (S_1 - S_6) )</td>
<td>( 8 (S_1 - S_8) )</td>
<td>( 5 (S_1 - S_5) )</td>
<td>( 6 (S_1 - S_6) )</td>
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<td>Voltage stresses of switches (( V_{ds,(0)} )) and diodes (( V_{ds,(0)} ))</td>
<td>( V_{ds,(3,5,6)} = V_o ) ( G )</td>
<td>( V_{ds,(1,2)} = V_o ) ( G )</td>
<td>( V_{ds,(1,2)} = V_o ) ( G )</td>
<td>( V_{ds,(1,4)} = V_o ) ( G )</td>
<td>( V_{ds,(1,4)} = V_o ) ( G )</td>
<td>( V_{ds,(1,4)} = V_o ) ( G )</td>
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<td>Current stresses of switches (( I_{ds,(0)} )) and diodes (( I_{ds,(0)} ))</td>
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<td>( I_{s,(1,2)} = I_o (1 + G) )</td>
<td>( I_{s,(1,4)} = I_o (1 + G) )</td>
<td>( I_{s,(1,4)} = I_o (1 + G) )</td>
<td>( I_{s,(1,4)} = I_o (1 + G) )</td>
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<tr>
<td>High-frequency switches/diodes</td>
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<td>Inductors</td>
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<td>Inductors peak current</td>
<td>( L_{s1} )</td>
<td>( L_{s1} )</td>
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<td>( L_{s1} )</td>
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<tr>
<td>Leakage reported efficiency (%)</td>
<td>96.8 at 800 W and 40 kHz</td>
<td>87 at 300 W and 10 kHz</td>
<td>86.3 at 300 W and 20 kHz</td>
<td>92.6 at 300 W and 20 kHz</td>
<td>93.7 at 800 W and 50 kHz</td>
<td>97.5 at 500 W and 50 kHz</td>
<td>97.5 at 500 W and 50 kHz</td>
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</table>

(*) ‘n’ in the subscript represent the switch/diode numbers.

The experiment results confirm that only HF switches \( S_1 \) and \( S_2 \) have voltage stresses equal to \( V_{in} + V_o \). The voltage stresses of LF switches are low and equal to the peak output voltage \( V_o \). Similarly, it can be observed that voltages across the parasitic capacitances are similar, as listed in Table I. During \( V_o > 0 \), the leakage currents are almost zero because both \( v_{p1} \) and \( v_{p2} \) are clamped to dc values. On the other hand, during \( V_o < 0 \), \( v_{p1} \) and \( v_{p2} \) vary with line frequency, and their high-frequency ripples are significantly attenuated by the filter capacitor \( C_o \). Therefore, small leakage currents exist during the negative portion of output voltage, but they are well below the industrial standards of 300 mA. The maximum leakage currents measured during the step-up and the step-down modes are about 75 mA and 45 mA, respectively.

The efficiency and total harmonic distortions (THD) of the output voltage are measured at 500 W for various input voltages, and the results are plotted in Fig. 18(a). The measured THD is much below the IEEE-519 limits throughout the voltage range, and a peak efficiency of 97.5% is achieved at \( V_{in} = 160 \) V. Similarly, efficiency is measured under different output power with constant output voltage and changing the load resistor. The graph of efficiency versus output power for two different input voltages is plotted in Fig. 18(b). While keeping output voltage constant, switching losses are more dominant than conduction losses at low power. However, the conduction losses increase with increasing power and eventually become dominant. Due to this reason, as presented in Fig. 18(b), the efficiency in the step-up mode is higher than the step-down mode in low power region. However, the efficiency in the step-down mode becomes better than the step-up mode at high power region.

Finally, detailed comparison of the proposed inverter with the well-known conventional buck-boost inverters which are good in terms of leakage current are included in Table III. It can be observed that apart from proposed and virtual-ground buck-boost inverter [21], all the other inverters require two inductors for buck-boost function with the same peak current ratings. However, the inverter in [21] still need two filter capacitors and hence it can be concluded that the proposed inverter has the fewest number of passive components (inductors and capacitors) which make it good in terms of power density. The proposed inverter has six semiconductor devices and only differential boost inverter [18] is good in terms of semiconductor count. However, all of the switches in [18] operate at HF and has high voltage and current stresses. In proposed inverter, only two switches with the same voltage and current stresses like [18] operate at HF. The other four switches in proposed inverter operate at LF and have low voltage and current stresses. The less number of passive components and HF switches make the proposed inverter quite good in terms of efficiency as well which is evident from the Table III.

V. MODULATION SCHEMES, DESIGN GUIDELINES, AND SIMULATION RESULTS OF THE PROPOSED INVERTERS (II-IV)

The proposed inverters (Types II-IV) have high voltage gain capabilities and can generate a high output voltage at small values of duty ratios. As mentioned earlier, the working principle of all the proposed inverters is similar; that is, the step-up cell is responsible for generating a full-wave rectified sinusoidal voltage with a dc-offset equal to the input voltage across the output capacitor \( C_o \). Furthermore, the switching devices \( S_a \) and \( S_d \) are ON for only the positive half of the
output voltage, while the switching devices \( S_b \) and \( S_c \) are ON for only the negative half of the output voltage in all the proposed inverters. The output voltage \( v_o \) and the voltage \( v_c \) of capacitor \( C_o \) are represented by the equations presented in (1) and (2), respectively. In order to generate \( v_c = V_{in} + |V_o \sin \omega t| \), the switching devices of the step-up cell of the proposed inverters (Type II-IV) are operated at HF through proper modulation schemes as follows.

A. Operation of the step-up cell of Type II inverter

The operating modes of Type II inverter are similar to Type I inverter, which are presented in Fig. 4(b). In modes 1 and 3, the switching device \( S_1 \) is ON, and the inductors \( L_1 \) and \( L_2 \) store energy from the input source \( V_{in} \) through the diodes \( D_1 \) and \( D_2 \) respectively as presented in Fig. 19(a). In modes 2 and 4, the switching device \( S_1 \) is OFF and the inductors \( L_1 \) and \( L_2 \) appear in series and charge the output capacitor \( C_o \) by \( D_3 \) as demonstrated in Fig. 19(b). By applying volt-second balance condition on inductors \( L_1 \) and \( L_2 \), the voltage on the capacitor \( C_o \) can be derived, which is given by

\[
v_c = V_{in} + V_o |\sin \omega t| = \frac{V_{in} (1 + d_1)}{1 - d_1}.
\]

(25)

Where \( d_1 \) is the duty ratio of the switching device \( S_1 \). Rearranging (25), \( d_1 \) can be written in terms of voltage gain

\[
G = \frac{v_o}{V_{in}}
\]

is given by:

\[
d_1 = \frac{G (|\sin \omega t|)}{2 + G (|\sin \omega t|)}.
\]

(26)

The maximum duty ratio \( D_{1,max} \) of switch \( S_1 \) can be obtained from (26) and is given by:

\[
D_{1,max} = \frac{G}{2 + G}.
\]

(27)

Using (27), the voltage gain \( G \) can be expressed in terms of \( D_{1,max} \) as presented in (28):

\[
G = \frac{v_o}{V_{in}} = \frac{2D_{1,max}}{1 - D_{1,max}}.
\]

(28)

B. Operation of the step-up cell of Type III inverter

The operating modes of Type III inverter are also similar to Type I inverter, which are presented in Fig. 4(b). In modes 1 and 3, the switching device \( S_1 \) is ON and the magnetizing inductor \( L_m \) is charged by the voltage contributed by the input source \( V_{in} \) and winding \( N_2 \) as presented in Fig. 20(a). In modes 2 and 4, the switching device \( S_1 \) is OFF and the switching device \( S_2 \) is ON. The windings \( N_1 \) and \( N_3 \) in series charge the capacitor \( C_o \) and the magnetizing inductor \( L_m \) is discharged through the winding \( N_2 \) directly and winding \( N_3 \) indirectly through coupling as presented in Fig. 20(b). It should be noted here that the lossless diode \( D_{sn} \) performs voltage clamping when the switching device \( S_2 \) is turned OFF by providing a path for the current of leakage inductance \( L_{lkg2} \) of winding \( N_2 \) to freewheel to the capacitor \( C_o \). On the other hand, if both HF complementary switches \( S_1 \) and \( S_2 \) are OFF during the small dead-time interval, the current of leakage inductances \( L_{lkg1} \) and \( L_{lkg3} \) of windings \( N_1 \) and \( N_3 \) can flow through the body diode of \( S_2 \) to energize the capacitor \( C_o \) and do not require extra diodes or snubbers for voltage clamping. By applying voltage-second balance condition on magnetizing inductor \( L_m \), the voltage on the capacitor \( C_o \) can be derived, which is given by

\[
v_c = V_{in} + V_o |\sin \omega t| = \frac{V_{in} \left[ 1 + \frac{N_1 + N_3}{N_1 - N_2} \right]}{1 - d_1}.
\]

(29)

Where \( d_1 \) is the duty ratio of the switching device \( S_1 \). Rearranging (29), \( d_1 \) can be written in terms of voltage gain

\[
G = \frac{v_o}{V_{in}}
\]

is given by

\[
d_1 = \frac{G (|\sin \omega t|)}{\left( \frac{N_1 + N_3}{N_1 - N_2} \right) + G (|\sin \omega t|)}.
\]

(30)

The maximum duty ratio \( D_{1,max} \) of switch \( S_1 \) can be obtained from (30) and is given by

\[
D_{1,max} = \frac{\left( \frac{N_1 + N_3}{N_1 - N_2} \right) + G}{G}.
\]

(31)

Using (31), the voltage gain \( G \) can be expressed in terms of \( D_{1,max} \) as presented in (32):

\[
G = \frac{v_o}{V_{in}} = \frac{D_{1,max} \left( \frac{N_1 + N_3}{N_1 - N_2} \right)}{1 - D_{1,max}}.
\]

(32)

C. Operation of the step-up cell of Type IV inverter

The gate signals and modes of operation of Type IV inverter are presented in Fig. 21. The switching devices \( S_1 \) and \( S_2 \) are operated at the same duty ratios; however, their gate signals are interleaved, which means a phase shift of 180° is included in their carrier signals. The gate signals of the switching device \( S_3 \) is complementary to switch \( S_1 \) while the gate signals of the switching device \( S_4 \) is complementary to switch \( S_2 \). Modes 1 – 4 appear in the positive half of the output voltage, while modes 5 – 8 appear in the negative half of the output voltage. The operation of LF switches \( S_{9-8} \) are exactly similar to that of inverter Type I, while high-frequency switches \( (S_1 - S_8) \) of the step-up cell are operated through a proper modulation scheme in order to obtain \( v_c = V_{in} + |V_o \sin \omega t| \).
In modes 1 and 5, the switching devices $S_1$ and $S_4$ are ON while the switching devices $S_2$ and $S_3$ are OFF. The inductor $L_1$ stores energy from the input source $V_{in}$ while the inductor $L_2$ and capacitor $C_1$ supply energy to the output capacitor $C_o$ as presented in Fig. 22(a). In modes 2 and 6, the switching devices $S_3$ and $S_4$ are ON, whereas the switching devices $S_1$ and $S_2$ are OFF. Both inductors ($L_1$, $L_2$) and capacitor $C_1$ supply energy to the output capacitor $C_o$ as presented in Fig. 22(b). In modes 3 and 7, the switching devices $S_1$ and $S_3$ are ON while the switching devices $S_2$ and $S_4$ are OFF. The inductor $L_2$ stores energy from the input source $V_{in}$ while the capacitor $C_1$ is charged by the current flowing through the inductor $L_1$ as presented in Fig. 22(c). The switching devices $S_1$ and $S_2$ are ON in modes 4 and 8, whereas the switching devices $S_3$ and $S_4$ are OFF. Both inductors $L_1$ and $L_2$ are charged by the input source $V_{in}$ while the capacitor $C_1$ is neither charged nor discharged, as presented in Fig. 22(d). It should be noted here that modes 4 and 8 appear only if the duty ratios of switches $S_1$ and $S_2$ are greater than 0.5. Similarly, modes 2 and 6 appear only if the duty ratios of switches $S_1$ and $S_2$ are smaller than 0.5. By applying voltage-second balance condition on inductors $L_1$ and $L_2$, the voltage on capacitor $C_o$ can be derived as in (33):

$$v_c = V_{in} + V_o|\sin \omega t| = \begin{cases} \frac{V_{in}}{1 - d_1} & \text{if } d_1 < 0.5 \\ \frac{2V_{in}}{1 - d_1} & \text{if } d_1 \geq 0.5 \end{cases} \quad (33)$$

Where $d_1$ is the duty ratio of the switching device $S_1$ and is equal to the duty-ratio $d_2$ of switch $S_2$ as explained earlier. Rearranging (33), $d_1$ can be expressed in terms of voltage gain:

$$d_1 = \begin{cases} \sqrt{1 + G|\sin \omega t| - 1} & \text{if } d_1 < 0.5 \\ \frac{G|\sin \omega t| - 1}{1 + G|\sin \omega t|} & \text{if } d_1 \geq 0.5 \end{cases} \quad (34)$$

The maximum duty ratio $D_{1,max}$ of switch $S_1$ can be obtained from (34) and is given by

$$D_{1,max} = \begin{cases} \sqrt{1 + G - 1} & \text{if } D_{1,max} < 0.5 \\ \frac{G - 1}{1 + G} & \text{if } D_{1,max} \geq 0.5 \end{cases} \quad (35)$$

Using (35), the voltage gain $G$ can be expressed in terms of $D_{1,max}$ as in (36):

$$G = \frac{V_o}{V_{in}} = \begin{cases} \frac{D_{1,max}(2 - D_{1,max})}{1 + D_{1,max}} + 1 & \text{if } D_{1,max} < 0.5 \\ \frac{1 + D_{1,max}}{1 - D_{1,max}} & \text{if } D_{1,max} \geq 0.5 \end{cases} \quad (36)$$

D. Components design guidelines

The selection of input capacitor $C_{in}$ and output capacitor $C_o$ of the inverters (Type II-IV) are similar to Type I inverter and are represented by (20) and (24), respectively. The normalized maximum drain-source voltages and the normalized peak current flowing through the inverters ($S_o$ - $S_a$) are also similar to Type I inverter and are given by (14) and (19), respectively. The normalized values for voltage stresses for Type II inverter's high-frequency diodes and switches are presented in (37):

$$\begin{align*}
V_{ds-1} &= \frac{V_{ds-2}}{V_0} = \frac{1 + G}{G} \\
V_{D1} &= \frac{V_{D2}}{V_0} = \frac{1}{2} \\
V_{D3} &= \frac{V_o}{V_0} = \frac{1}{G}
\end{align*} \quad (37)$$

Where $V_{ds-1}$ and $V_{ds-2}$ represent the voltage stresses of the switching devices $S_1$ and $S_2$ while $V_{D1}$, $V_{D2}$, and $V_{D3}$ represent the voltage stresses of the diodes $D_1$, $D_2$, and $D_3$.

Similarly, the maximum current flowing through the diodes and switches of Type II inverter are normalized to the peak output current $I_o$ and are calculated as follows

$$\begin{align*}
\frac{I_{D1}}{I_o} &= \frac{I_{D2}}{I_o} = \frac{I_{D3}}{I_o} = \frac{I_{D2}}{I_o} = \frac{2 + G}{2} \\
\frac{I_{S1}}{I_o} &= \frac{2 + G}{2}
\end{align*} \quad (38)$$

Where $I_{D1}$, $I_{D2}$, $I_{D3}$, $I_{S1}$, and $I_{S2}$ represent the maximum current flowing through the diodes $D_1$, $D_2$, $D_3$ and switches $S_1$ and $S_2$, respectively.

The current handling requirements ($I_{L1}$, $I_{L2}$) of inductors $L_1$ and $L_2$ are given by
Voltage gain $G$ inverter are given by

$$L = \frac{V_{in} T_g G}{L_2 (2 + G)}.$$  \hspace{1cm} \text{Type II} \hspace{1cm} (40)$$

Where \(\Delta_i_{1,\text{max}} = \Delta_i_{2,\text{max}} = yL_{1} = yL_{2}\), and \(y = 10\% \) to 50\%. Putting these values and \((39)\) in \((40)\), the formula for inductances \(L_1\) and \(L_2\) can be calculated as follows

$$L_1 = L_2 = \frac{2V_{in} T_g}{y(2 + G)^2 I_o} = \frac{2V_o T_g}{yL_o(2 + G)^2}.$$  \hspace{1cm} \text{Type II} \hspace{1cm} (41)$$

The normalized voltage and current stresses of HF switches and diodes of Type III and IV inverters can be derived similarly and are as follows.

$$\begin{align*}
V_{ds-1} &= \frac{1 + G}{G}, & \text{if } G < 3 \\
V_{ds-2} &= \frac{1 + (N_1 + N_3)(N_1 - N_2)}{G(N_1 - N_2)}, & \text{if } G \geq 3 \\
I_{s1} &= \frac{I_{dsn}}{I_o} = (N_1 + N_3)(N_1 - N_2) + G \\
I_{s2} &= \frac{I_{dsn}}{I_o} = G(N_1 - N_2) \\
I_o &= \frac{1 + G}{N_1 + N_3}
\end{align*}$$

\hspace{1cm} \text{Type III} \hspace{1cm} (42)$$

$$\begin{align*}
V_{ds-2} &= \frac{\sqrt{1 + G}}{G}, & \text{if } G < 3 \\
V_{ds-4} &= \frac{1 + G}{2G}, & \text{if } G \geq 3 \\
V_{ds-3} &= \frac{1 + G}{G} \\
I_{s1} &= \frac{I_{dsn}}{I_o} = \sqrt{1 + G}. & \text{if } G < 3 \\
I_{s2} &= \frac{I_{dsn}}{I_o} = \frac{1 + G}{2}. & \text{if } G \geq 3 \\
I_o &= \frac{1 + G}{2} \\
I_{s4} &= \frac{1 + G}{I_o} & \text{if } G < 3 \\
I_o &= \frac{1 + G}{I_o} & \text{if } G \geq 3
\end{align*}$$

\hspace{1cm} \text{Type IV} \hspace{1cm} (45)$$

Finally, the aforementioned results are summarized in Table IV in order to briefly compare all the proposed topologies. The equations for voltage and current stresses of LF switches, output capacitor and input capacitor are similar for all the proposed inverters given by \((14)\), \((19)\), \((20)\), and \((24)\) and are not included in Table IV. The graph of voltage gain \(G\) versus maximum duty ratio \(D_{1,\text{max}}\) for the proposed inverters are plotted in Fig. 23. For the graph of type III inverter \(N_1: N_2: N_3\) is kept 2:1:2. Fig. 23 confirms that the proposed type II, III, and IV inverters have high voltage gain capabilities with the type III inverter having an additional degree of flexibility to achieve high voltage gain by adjusting the turns ratio of the coupled inductor. Type I inverter is suitable for applications when the input voltage can be both greater and smaller than the output voltage [9]-[15], [17]-[20], such as several PV panels connected to the grid. On the other hand, type II, III, and IV inverters are suitable for applications when the output voltage is substantially higher than the input voltage [25]-[30] such as a single PV panel connected to the grid. The graphs of normalized voltage and current stresses of the switching devices and diode (see Table IV) of the type I inverter are already shown in Fig. 9 while that of types II, III, and IV inverters are presented in Figs. 24 and 25. It can be observed that the voltage stresses of the switching devices and diodes of the proposed inverters decrease while their current stresses increase with the voltage gain \(G\). This implies that the voltage ratings for the devices and switching devices should be based on the minimum required value of \(G\) while the current ratings should be selected based on the maximum value of \(G\). Similarly, replacing \(V_{in} T_g / yI_o\) in Table IV by constant \(k\), the normalized inductances \((L / k)\) of the types II, III, and IV inverters are plotted in Fig. 26 while that of type I inverter is already presented in Fig. 10 earlier. The graphs imply that the value of inductance \(L\) should be chosen at the minimum voltage gain \(G\) because the inductance value is maximum at this point.
E. Simulation results and comparative analysis

In order to prove the working principle of the proposed inverters (Type II-IV), simulations are performed in PSIM with the electrical specifications mentioned in Table V. The waveforms of input voltage $V_{in}$, output voltage $v_o$, output current $i_o$, the voltage across the output filter capacitor $v_c$, and voltages across the parasitic capacitances $v_{p1}$ and $v_{p2}$ of the proposed Type II inverter are presented in Fig. 27. The simulation waveforms of Type III inverter are presented in Fig. 28, and the simulation waveforms of Type IV inverter are presented in Fig. 29. It can be observed that the voltages across the output filter capacitors of the inverters (Type II-IV) are rectified sinusoidal voltages with dc-offset equal to the input voltage. Similarly, voltages across the parasitic capacitances are either constant or vary sinusoidally with no significant high-frequency voltage variations, which agrees with the earlier theoretical analysis. A brief comparison of the proposed type II, III, and IV inverters are also made with the conventional high-gain topologies in Table VI. It can be observed that all the inverters in Table VI are capable of achieving high voltage gain. The inverters in [25] and [26] are good in terms of switch count but the high leakage current make it less effective. The inverter in [29] has small leakage current but the high number of active and passive components are the downside of this topology. The inverter in [30] is another promising topology with voltage gain exactly similar to that of the proposed type III inverter but it has only 50% magnetic utilization. Furthermore, all the proposed inverters have low leakage current due to their virtual-ground characteristics and have the least number of switches operating at high frequency which is good for achieving high efficiency and make it suitable for PV applications.

### Table IV. Comparison of the Proposed Topologies

<table>
<thead>
<tr>
<th>Proposed inverter</th>
<th>Voltage gain</th>
<th>$S^0$</th>
<th>$D^0$</th>
<th>$L^0$</th>
<th>$C^0$</th>
<th>Voltage stresses of switches &amp; diodes</th>
<th>Current stresses of switches &amp; diodes</th>
<th>Inductor current</th>
<th>Inductance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type I</td>
<td>$G = \frac{D_{1\max}}{1 - D_{1\max}}$</td>
<td>6</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>$V_{ds-1}, V_{ds-2} = 1 + \frac{G}{G}$</td>
<td>$I_{s1}, I_{s2} = 1 + G$</td>
<td>$I_o = (1 + G) \cdot I_o$</td>
<td>$L = \frac{V_{ds} I_o}{y(1 + G) T_o}$</td>
</tr>
<tr>
<td>Type II</td>
<td>$G = \frac{2D_{1\max}}{1 - D_{1\max}}$</td>
<td>6</td>
<td>3</td>
<td>2</td>
<td>2</td>
<td>$V_{ds-1}, V_{ds-2} = 1 + \frac{G}{G}$</td>
<td>$I_{ds-1} I_{ds-2} = 2 + G$</td>
<td>$I_o = \frac{(1 + G) I_o}{2}$</td>
<td>$L_{1\max}, L_2 = \frac{2V_{ds} I_o}{y(2 + G)^2}$</td>
</tr>
<tr>
<td>Type III</td>
<td>$G = \frac{D_{1\max} (N_1 + N_2)}{1 - D_{1\max}}$</td>
<td>6</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>$V_{ds-1}, V_{ds-2} = 1 + \frac{G}{G}$</td>
<td>$I_{ds-1} I_{ds-2} = 2 + G$</td>
<td>$I_o = \frac{(1 + G) I_o}{2}$</td>
<td>$L = \frac{V_{ds} I_o}{y(1 + G) T_o}$</td>
</tr>
</tbody>
</table>

(1) $S$: Number of switches. (2) $D$: Number of diodes. (3) $L$: Number of inductors. (4) $C$: Number of capacitors. (5) $CL$: Coupled inductor.

### Table V. Electrical Specifications of Type II, III, and IV Inverters

<table>
<thead>
<tr>
<th>Specification</th>
<th>Type II</th>
<th>Type III</th>
<th>Type IV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power</td>
<td>250 W</td>
<td>500 W</td>
<td>500 W</td>
</tr>
<tr>
<td>Input voltage $V_{in}$</td>
<td>30 $V_{dc}$</td>
<td>30 $V_{dc}$</td>
<td>30 $V_{dc}$</td>
</tr>
<tr>
<td>Output voltage $v_o$</td>
<td>355 $V_{peak}$</td>
<td>355 $V_{peak}$</td>
<td>355 $V_{peak}$</td>
</tr>
<tr>
<td>Inductors $L_1, L_2$</td>
<td>200 $\mu H$</td>
<td>200 $\mu H$</td>
<td>200 $\mu H$</td>
</tr>
<tr>
<td>Magnetizing inductor $L_{m}$ (type III)</td>
<td>250 $\mu H$</td>
<td>250 $\mu H$</td>
<td>250 $\mu H$</td>
</tr>
<tr>
<td>Inductors $L_1, L_2$ (type IV)</td>
<td>200 $\mu H$</td>
<td>200 $\mu H$</td>
<td>200 $\mu H$</td>
</tr>
<tr>
<td>Capacitor $C_1$ (Type IV)</td>
<td>5 $\mu F$</td>
<td>5 $\mu F$</td>
<td>5 $\mu F$</td>
</tr>
<tr>
<td>Capacitor $C_o$</td>
<td>5 $\mu F$</td>
<td>5 $\mu F$</td>
<td>5 $\mu F$</td>
</tr>
<tr>
<td>Parasic capacitances $C_{p1}, C_{p2}$</td>
<td>50 $nF$</td>
<td>50 $nF$</td>
<td>50 $nF$</td>
</tr>
</tbody>
</table>

### Fig. 24. Graph of the normalized voltage stresses versus voltage gain of the proposed inverters (Type II-IV).

### VI. CONCLUSION

In this article, a new family of single-phase transformerless buck-boost inverters is proposed. The family includes four types of inverters (Type I-IV). The proposed Type I Inverter has a wide gain range, while Types II, III, and IV are capable of achieving high voltage gain at small duty ratios. These
ininverters possess virtual-ground characteristics, which makes them efficient in terms of leakage current. Additionally, four of the switching devices in the proposed inverters operate at low frequencies and have low voltage and current stresses. This feature is beneficial in terms of efficiency, as it reduces switching losses. The performance of the proposed inverters is supported by detailed theoretical analysis, simulations, and experiment results, which demonstrate their effectiveness.

![Graph of normalized current stresses versus voltage gain of the proposed inverters (Type II-IV).](image)

![Graph of normalized inductances versus voltage gain of the proposed inverters (Type II-IV).](image)

### Table VI. Comparison of the proposed type II, III, and IV inverters with conventional high-gain inverters.

<table>
<thead>
<tr>
<th>Topology</th>
<th>[25]</th>
<th>[26]</th>
<th>[29]</th>
<th>[30]</th>
<th>Proposed type II</th>
<th>Proposed type III</th>
<th>Proposed type IV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage gain ($G^*$)</td>
<td>$\frac{1}{1 + \frac{nD_{bat}}{1 - D_{bat}}}$</td>
<td>$\frac{(k + 1)(2D - 1)}{D(1 - D)}$</td>
<td>$\frac{D(N_1 + N_2)}{N_1(1 - D)}$</td>
<td>$G = \frac{2D}{1 - D}$</td>
<td>$G = \frac{D(N_1 + N_2)}{N_1(1 - D)}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switches</td>
<td>5</td>
<td>4</td>
<td>8</td>
<td>4</td>
<td>6</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td>Diodes</td>
<td>3</td>
<td>3</td>
<td>0</td>
<td>2</td>
<td>3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Inductors (L) / Coupled inductors (CL)</td>
<td>2 (1 L and 1 CL)</td>
<td>2 (1 L and 1 CL)</td>
<td>2 L</td>
<td>2 CL</td>
<td>2 L</td>
<td>1 CL</td>
<td>2 L</td>
</tr>
<tr>
<td>Capacitors</td>
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<td>6</td>
<td>3</td>
<td>2</td>
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<td>3</td>
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<tr>
<td>Line-frequency switches</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>High-frequency switches</td>
<td>5</td>
<td>4</td>
<td>8</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Leakage current</td>
<td>High</td>
<td>High</td>
<td>small</td>
<td>small</td>
<td>small</td>
<td>small</td>
<td>small</td>
</tr>
</tbody>
</table>

(*) 'n' represents turns ratio of the coupled inductor; 'D' represents the peak of value of duty ratio of sinusoidal pwm scheme; 'D_{bat}' is constant and it represent the duty ratio of the integrated boost converter; 'k' represents the number of multiplier cell.

![Fig. 27. Simulation waveforms of type II inverter. (a) Input voltage $V_{in}$. (b) Output current $i_o$. (c) Voltage across output filter capacitor $v_{C}$. (d) Voltages across parasitic capacitances $v_{p1}$ and $v_{p2}$.](image)

![Fig. 28. Simulation waveforms of type III inverter. (a) $V_{in}$ and $v_o$. (b) Output current $i_o$. (c) Voltage $v_c$. (d) Voltages $v_{p1}$ and $v_{p2}$.](image)

![Fig. 29. Simulation waveforms of type IV inverter. (a) $V_{in}$ and $v_o$. (b) Output current $i_o$. (c) Voltage $v_c$. (d) Voltages $v_{p1}$ and $v_{p2}$.](image)

### REFERENCES


