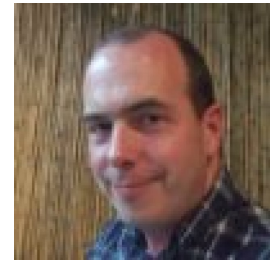


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Research Interests

Roger is a member of the AI Research Theme. His research interests includes:

Novel computing systems including multi-precision computing, edge computing solutions, Field Programmable Gate Arrays

Big Data analytics particularly focused at manufacturing.

Innovative telecommunications hardware platforms incorporating edge AI technology for advanced security and IoT applications.

Research output

Optimisation of System Throughput Exploiting Tasks Heterogeneity on Space Shared FPGAs

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Novel Network Functionality for Interactive layered MPEG-4 Video Conferencing

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Rapid Generation of Hardware Functionality in Heterogeneous Platforms

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Gocan, S., O'Neill, M., Paar, C. & Woods, R., 2005, In : IEE Proc. on Information Security. 1, p. 1-2 2 p.

LMS Coefficient Filtering for Time-Varying Chirped Signals

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Highly efficient, limited range multipliers for LUT-based FPGA architectures

Turner, R. & Woods, R., Oct 2004, In : IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 12(10), 10, p. 1113-1118 6 p.

Synthesis and High Level Optimisation of Multidimensional Dataflow Actor Network on FPGA

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Design Technologies for DSP Algorithm Implementation on Heterogeneous Architectures

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Hierarchical DSP architectural synthesis and scheduling solution for "IRIS"

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Design flow for efficient FPGA reconfiguration

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Development of a Run-Time Reconfiguration System with Low Reconfiguration Overhead

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Low-power synthesis flow for regular processor design

Woods, R., Lightbody, G., Cassidy, A., Gareth, K. & Spanier, J., Jan 2001. 12 p.

Low-power synthesis flow for regular processor design

Woods, R., Lightbody, G., Cassidy, A., Keane, G. & Spanier, J., 2001, *Unified low-power design flow for data dominated multi-media and telecom applications*. Springer-Verlag

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Advances in adaptive signal processing: Totally adaptive systems

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An investigation of reconfigurable multipliers for use in adaptive signal processing

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Low Power Implementation of a Discrete Cosine Transform IP core

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Rapid Design of a Single Chip Adaptive Beamformer"

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Multiplexer based reconfiguration for virtex multipliers

Courtney, T., Turner, R. & Woods, R., 01 Jan 2000, In : *Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics)*. 1896, p. 749-758 10 p.

Linear QR architecture for a single chip adaptive beamformer

Lightbody, G., Walke, R., Woods, R. & McCanny, J., 2000, In : *Journal of VLSI signal processing systems for signal, image and video technology*. 24, 1, p. 67-81 15 p.

A virtual hardware handler for RTR systems

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Real-Time Emulation of Fault Management functions within an SDH Network

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Architectural synthesis of an image processing algorithm using IRIS

Trainor, D. W., Woods, R. F. & McCanny, J. V., 01 Jan 1995, *IEEE VLSI Signal Processing VIII, IEEE Signal Processing Soc. ed. T Nishitani, K Pahari*. p. 167-176 10 p.

High performance IIR filter chip and its evaluation system

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Real-Time modelling of Alarm Generation and Propagation in an SDH Network

Hayes, P., Marshall, A. & Woods, R., Nov 1994, p. 921-926. 6 p.

Novel VLSI implementation of (8×8) point 2-DDCT

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High performance DSP ASIC for multiply, divide and square root

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The design of a VLSI array processor chip for computing the basic arithmetic operations

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Saturation circuitry for redundant number based hr filters

Woods, R. F., McNally, O. C. & Mcquillan, S., 10 Oct 1991, In : *Electronics Letters*. 27, 21, p. 1961-1963 3 p.

High performance VLSI architecture for division and square root

McQuillan, S. E., McCanny, J. V. & Woods, R. F., 01 Jan 1991, In : *Electronics Letters*. 27, 1, p. 20-21 2 p.

VLSI Systems for DSP and Control

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Optimized bit level architectures for IIR filtering

McNally, O. C., McCanny, J. V. & Woods, R. F., 01 Sep 1990, *Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors*. LOS ALAMITOS: IEEE Computer Society, p. 302-306 5 p.

Bit-Level systolic architectures for high performance IIR filtering

Knowles, S. C., McWhirter, J. G., Woods, R. F. & McCanny, J. V., 01 Aug 1990, In : *Journal of VLSI signal processing systems for signal, image and video technology*. 1, 1, p. 9-24 16 p.

Pipelined two-port adaptor for wave digital filtering

Singh, R. J., McCanny, J. V. & Woods, R. F., 01 Jan 1990, In : *ICASSP, IEEE International Conference on Acoustics, Speech and Signal Processing - Proceedings*. 2, p. 1033-1036 4 p.

Systolic array architectures for parameterised multiplexed IIR filters

Woods, R. F., McGovern, B. P. & McCanny, J. V., 01 Jan 1990, In : *IEE Colloquium (Digest)*. 95

A high performance IIR digital filter chip

Woods, R. F., McCanny, J. V., Knowles, S. C. & McNally, O. C., 1990, *Proceedings - IEEE International Symposium on Circuits and Systems*. NEW YORK: Ashgate Publishing, Vol. 2. p. 1410-1413 4 p.

Bit-level systolic architecture for very high performance IIR filters

Knowles, S. C., McWhirter, J. G., Woods, R. F. & McCanny, J. V., 01 Jan 1989, In : *ICASSP, IEEE International Conference on Acoustics, Speech and Signal Processing - Proceedings*. 4, p. 2449-2452 4 p.

A high performance systolic IIR filter architecture

Knowles, S., Woods, R., McWhirter, J. & McCanny, J. V., 15 Dec 1988, *IEE Colloquium on Digital Signal Processing for VLSI*.

Bit-level systolic arrays for IIR filtering.

Knowles, S. C., Woods, R. F., McWhirter, J. G. & McCanny, J. V., 01 Jan 1988, *IEEE Computer Society Press, Intl. Conf. on Systolic Arrays*, eds. K Bromley, E S Swartzlander Jr and S Y Kung. p. 653-663 11 p.

Systolic building block for high performance recursive filtering

Woods, R. F., Knowles, S. C., McCanny, J. V. & McWhirter, J. G., 01 Jan 1988, *Proceedings - IEEE International Symposium on Circuits and Systems*. Vol. 3. p. 2761-2764 4 p.

SYSTOLIC IIR FILTERS WITH BIT LEVEL PIPELINING.

Woods, R. F., Knowles, S. C., McCanny, J. V. & McWhirter, J. G., 01 Jan 1988, In : *ICASSP, IEEE International Conference on Acoustics, Speech and Signal Processing - Proceedings*. p. 2072-2075 4 p.

Projects

R1898ECI: Adaptive Hardware Systems with Novel Algorithmic Design and Guaranteed Resource Bounds

Woods, R.
01/08/2007 → ...

R1701ECI: CASE award: M.S. Mckeown- EPSRC/SELEX

Woods, R.
01/08/2005 → ...

R1848ELE: Dorothy Hodgkin Postgraduate Award

Woods, R.
01/08/2006 → ...

R1318ECI: eFUTURES XD

Woods, R.
01/08/2011 → 27/05/2015

R1057ECI: eFutures2 : exploiting the UK's rich heritage in electronics

Woods, R.
15/04/2019 → ...

R1337CSC: ENPOWER

Nikolopoulos, D. & Woods, R.
01/08/2013 → 05/02/2018

R1603ELE: EPSRC Case Ref 0430024 - Hasson

Woods, R.
01/08/2004 → ...

R1917CNR: Health Data Research UK (HDR UK)

Lawler, M., Blayney, J., Coleman, H., Dunne, P., Heaney, L., Kee, F., McArt, D., Nikolopoulos, D., O'Reilly, D., Overton, I., Salto-Tellez, M. & Woods, R.
29/10/2018 → ...

R1129ECI: Kelvin-2 - The High Performance Computing Centre in Northern Ireland (HPC-NI)

Woods, R., Chevallier, O., Gillan, C., Hu, P., Rafferty, K., Salto-Tellez, M., Tikhonova, I. & Vandierendonck, H.

04/12/2019 → ...

R6410CSC: NanoStreams: A Hardware and Software Stack for Real-Time Analytics on Fast Data Streams

Nikolopoulos, D., Spence, I. & Woods, R.

01/08/2013 → ...

R6551CSC: Open TransPREcision COMPuting

Woods, R., Karakonstantis, G. & Vandierendonck, H.

03/11/2016 → ...

R1138ECI: Programmable embedded platforms for remote and compute intensive image processing applications

Woods, R.

01/08/2012 → 31/07/2017

R1722CMM: Queen's University Belfast Imaging and Patterning Centre

Gregg, M., McNeill, D., Mitchell, N. & Woods, R.

20/02/2017 → 31/03/2018

R1728ELE: SHARES- System-on-chip heterogeneous architecture recognition engine for speech

Woods, R. & Ji, M.

01/08/2005 → ...

R1128CSC: Softcore Streaming Processors for FPGA DSP

McAllister, J. & Woods, R.

01/08/2009 → 28/02/2014

R1917ECI: Support for International Workshop on Applied Reconfigurable Computing in 2008

Woods, R.

01/08/2007 → ...

R1307ECI: WifiEar: A New Form of Telecoil

Woods, R. & Marshall, A.

01/08/2012 → ...

Awards

Activities

Meeting The Challenges of an Ageing Society

Roger Woods (Advisor)

17 Feb 2020

Big Data conference

Roger Woods (Participant)

24 Oct 2019

15th International Symposium on Applied Reconfigurable Computing

Roger Woods (Conference committee co-chair)

01 May 2019

Big Data Week

Roger Woods (Chair)

18 Oct 2018

26th European Signal Processing Conference
Roger Woods (Member of programme committee)
03 Sep 2018 → 07 Sep 2018

International Conference on Field Programmable Logic and Applications
Roger Woods (Member of the organising committee)
27 Aug 2018 → 31 Aug 2018

UK Research and Innovation (External organisation)
Roger Woods (Advisor)
20 Aug 2018 → ...

IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation
Roger Woods (Member of programme committee)
15 Jul 2018 → 19 Jul 2018

14th International Symposium on Applied Reconfigurable Computing (Event)
Roger Woods (Board Member)
02 May 2018

Big Data conference
Roger Woods (Chair)
19 Oct 2017

Big Data Week
Roger Woods (Chair)
17 Oct 2017

IEEE International Workshop on Signal Processing Systems
Roger Woods (Member of programme committee)
03 Oct 2017 → 05 Oct 2017

FPL2017
Roger Woods (Member of programme committee)
04 Sep 2017 → 08 Sep 2017

17th International Conference on Embedded Computer Systems: Architectures, Modelling and Simulation
Roger Woods (Participant)
17 Jul 2017 → 20 Jul 2017

eFutures Annual Community Event
Roger Woods (Participant)
23 May 2017

International Symposium on Applied Reconfigurable Computing
Roger Woods (Member of programme committee)
03 Apr 2017 → 07 Apr 2017

IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Journal)
Roger Woods (Peer reviewer)
14 Mar 2017

FPL2017

Roger Woods (Advisory board member)
2017

Key Generation from Wireless Channels

Roger Woods (Invited speaker), Alan Marshall (Invited speaker), & Junqing Zhang (Invited speaker)
08 Dec 2016

Key Generation from Wireless Channels

Roger Woods (Invited speaker)
04 Dec 2016 → 08 Dec 2016

IEEE International Workshop on Signal Processing Systems

Roger Woods (Member of programme committee)
26 Oct 2016 → 28 Oct 2016

International Conference on Field-Programmable Logic and Applications

Roger Woods (Member of programme committee)
29 Aug 2016 → 02 Sep 2016

16th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation

Roger Woods (Member of programme committee)
17 Jul 2016 → 21 Jul 2016

16th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, SAMOS 2016

Roger Woods (Member of programme committee)
17 Jul 2016 → 21 Jul 2016

Big Data Week

Roger Woods (Chair)
02 Jun 2016

Big Data conference

Roger Woods (Chair)
20 May 2016

International Conference on Field-Programmable Logic and Applications

Roger Woods (Advisory board member)
2016

IEEE International Workshop on Signal Processing Systems

Roger Woods (Member of programme committee)
14 Oct 2015 → 16 Oct 2015

International Conference on Field-Programmable Logic and Applications

Roger Woods (Member of programme committee)
02 Sep 2015 → 04 Sep 2015

IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation

Roger Woods (Member of programme committee)
20 Jul 2015 → 23 Jul 2015

FPGA-based acceleration of data applications

Roger Woods (Advisor)
11 May 2015

Big Data Conference

Roger Woods (Chair)
23 Apr 2015

48th Asilomar Conference on Signals, Systems and Computers

Roger Woods (Chair)
02 Nov 2014 → 05 Nov 2014

IEEE Workshop on Signal Processing Systems

Roger Woods (Member of the organising committee)
22 Oct 2014 → 24 Oct 2014

Entrepreneurship in practice in a university setting

Roger Woods (Advisor)
16 Oct 2014

WiPhyLoc8: VLSI Algorithms and Architectures for Positioning and Security in Wireless Communication Systems

Roger Woods (Advisor)
06 Oct 2014

Workshop on FPGA-based Implementation of Signal Processing Systems

Roger Woods (Participant)
23 Jun 2014 → 27 Jun 2014

Big Data Week

Roger Woods (Chair)
07 May 2014

Research Excellence Framework (REF) (External organisation)

Roger Woods (Member)
2014

IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation

Roger Woods (Vice chair)
15 Jul 2013 → 18 Jul 2013

Engineering & Physical Sciences Research Council (External organisation)

Roger Woods (Chair)
29 May 2013

Engineering & Physical Sciences Research Council (External organisation)

Roger Woods (Member)
06 Feb 2013

Novel architectures and design tools for the implementation of complex DSP systems on FPGA-based technologies

Roger Woods (Speaker)
08 Nov 2012

IEEE Signal Processing Summer School

Roger Woods (Organiser)
20 Aug 2012 → 24 Aug 2014

Research Excellence Framework (REF) Panel (External organisation)

Roger Woods (Member)
01 Apr 2011 → 31 Dec 2014

International Workshop on Applied Reconfigurable Computing

Roger Woods (Chair)
23 Mar 2011 → 25 Mar 2011

Engineering Policy Group Northern Ireland (External organisation)

Roger Woods (Vice Chair)
2011 → ...

EPSRC Associate Peer Review College (External organisation)

Roger Woods (Member)
2011 → ...

eFutures (External organisation)

Roger Woods (Board Member)
2010 → ...

Microelectronics Design Grand Challenges: uGC1: Batteries Not Included

Roger Woods (Member)
23 Nov 2009

International Conference on Wireless Communications and Signal Processing, Nanjing, China

Roger Woods (Keynote/plenary speaker)
13 Nov 2009

17th European Signal Processing Conference (EUSIPCO-2009)

Roger Woods (Invited speaker)
27 Aug 2009

International Workshop on Applied Reconfigurable Computing

Roger Woods (Chair)
16 Mar 2009 → 18 Mar 2009

Analytics Engines Limited (External organisation)

Roger Woods (Board Member)
2007 → ...

IEEE Advisory board to the IEEE Signal Processing Society Technical Committee on the Design and Implementation of Signal Processing Systems (External organisation)

Roger Woods (Board Member)
2007 → ...

ACM Transactions on Reconfigurable Technology and Systems (Journal)

Roger Woods (Editorial board member)
2006

ACM Transactions on Reconfigurable Technology and Systems (Journal)

Roger Woods (Associate editor)
2005 → ...

EURASIP Journal on Signal Processing (Journal)

Roger Woods (Editorial board member)

2004 → 2007

Journal of VLSI signal processing systems for signal, image and video technology (Journal)
Roger Woods (Editorial board member)
2003 → ...

IET COMPUTERS AND DIGITAL TECHNIQUES (Journal)
Roger Woods (Associate editor)
2001 → ...

Press clippings

A conversation with Analytics Engines' and Queen's University's Roger Woods
Roger Woods
01/09/2017
1 Media contribution

Analytics Engines | Stephen McKeown | Invest NI Support
Roger Woods
08/05/2013
1 Media contribution

Big Data conference is a Titanic success
Roger Woods
20/10/2017
1 Media contribution