Research Interests
Roger is a member of the AI Research Theme. His research interests includes:

- Novel computing systems including multi-precision computing, edge computing solutions, Field Programmable Gate Arrays
- Big Data analytics particularly focused at manufacturing.
- Innovative telecommunications hardware platforms incorporating edge AI technology for advanced security and IoT applications.

Research output

**Optimisation of System Throughput Exploiting Tasks Heterogeneity on Space Shared FPGAs**

**Impact of Wireless Backhaul Unreliability and Imperfect Channel Estimation on Opportunistic NOMA**

**Physical Layer Security for the Internet of Things: Authentication and Key Generation**

**Evaluation of FPGA Partitioning Schemes for Time and Space Sharing of Heterogeneous Tasks**

**An Investigation of Using Loop-back Mechanism for Channel Reciprocity Enhancement in Secret Key Generation**

**FPGA-based Processor Acceleration for Image Processing Applications**

**Programmable Architectures for Histogram of Oriented Gradients Processing**

**Work-in-Progress: Design Space Exploration of Multi-Task Processing on Space Shared FPGAs**
Opportunistic Non-Orthogonal Multiple Access Scheme with Unreliable Wireless Backhauls

Facilitating Easier Access to FPGAs in the Heterogeneous Cloud Ecosystems

A New Data Analytics Framework Emphasising Pre-processing in Learning AI Models for Complex Manufacturing Systems

NanoStreams: A Microserver Architecture for Real-time Analytics on Fast Data Streams

Security Optimization of Exposure Region-based Beamforming with a Uniform Circular Array

A Bayesian network based learning system for modelling faults in large-scale manufacturing

Exploring Functional Acceleration of OpenCL on FPGAs and GPUs Through Platform-Independent Optimizations

On spatial security outage probability derivation of exposure region based beamforming with randomly located eavesdroppers

A New Real-Time FPGA-Based Implementation of K-Means Clustering for Images

Understanding complex interactions within a large-scale manufacturing system through applications of Bayesian networks

Securing Wireless Communications of the Internet of Things from the Physical Layer, An Overview

Angle of Arrival based Indoor Localization with Cooperative MIMO Beamforming Scheme
FPGA-based implementation of Signal Processing Systems

FPGA-based soft-core processors for image processing applications

On the Key Generation from Correlated Wireless Channels
Zhang, J., He, B., Duong, T. Q. & Woods, R., Apr 2017, In : IEEE Communications Letters. 21, 4, p. 961-964

Advanced computer technologies and their benefits for Bayesian network learning

On Spatial Security Outage Probability Derivation of Exposure Region Based Beamforming with Randomly Located Eavesdroppers

Design of an OFDM Physical Layer Encryption Scheme

Defining Spatial Security Outage Probability for Exposure Region Based Beamforming

NanoStreams: Codesigned Microservers for Edge Analytics in Real Time

Runtime Support for Adaptive Power Capping on Heterogeneous SoCs

Experimental Study on Key Generation for Physical Layer Security in Wireless Communications

Proposing the deep dynamic Bayesian network as a future computer based medical system

Experimental Study on Channel Reciprocity in Wireless Key Generation

Efficient Key Generation by Exploiting Randomness from Channel Responses of Individual OFDM Subcarriers
FPGA Soft-core Processors, Compiler and Hardware Optimizations validated using HOG

FPGA soft-core processors, compiler and hardware optimizations validated using HOG

Key Generation from Wireless Channels: A Review

Verification of Key Generation from Individual OFDM Subcarrier’s Channel Response

An effective key generation system using improved channel reciprocity

An effective key generation system using improved channel reciprocity

Secure key generation from OFDM subcarriers’ channel responses

Power Modeling and Capping for Heterogeneous ARM/FPGA SoCs

Secure Key Generation from OFDM Subcarriers’ Channel Response

Creating secure wireless regions using configurable beamforming

Investigation of secure wireless regions using configurable beamforming on WARP

Histogram of oriented gradients front end processing: An FPGA based processor approach
IPPro: FPGA based Image Processing Processor

Engineering Innovative Products: A Practical Experience

Dataflow toolset for soft-core processors on FPGA for image processing applications

Implementation of Selective Packet Destruction on Wireless Open-Access Research Platform

Optimization of Weighted Finite State Transducer for Speech Recognition

Mapping decidable signal processing graphs into FPGA implementations

Preface - ARC

An On Demand Queue Management Architecture for a Programmable Traffic Manager

Novel Application of Genetic Sequencing algorithms to optimisation of hardware resource sharing for DSP

A Low Complexity Real-time MIMO-Preprocessing For Fixed Complexity Sphere Decoder

Design and implementation of a flexible queue manager for next generation networks

Tree-Based Adaptive Spatial Detection for Adaptive Modulated MIMO Systems

Design of quantum-dot cellular automata circuits using cut-set retiming

Real-valued fixed-complexity sphere decoder for high dimensional QAM-MIMO systems
GPU acceleration of Automated Speech Recognition for Mobile Devices

A Scalable and Programmable Modular Traffic Manager Architecture

Lecture Notes in Computer Science (including subseries Lecture Notes in Artificial Intelligence and Lecture Notes in Bioinformatics): Preface

A Pipeline Interleaved Heterogeneous SIMD Soft Processor Array Architecture for MIMO-OFDM Detection

Reconfigurable Computing: Architectures, Tools and Applications

How resistant are SBoxes to Power Analysis Attacks?*,

Preface

FPGA based Soft-core SIMD Processing: A MIMO-OFDM Fixed-Complexity Sphere Decoder Case Study

Improvements in or relating to Pattern Recognition

Random Clock against Differential Power Analysis

Security of AES Sbox Designs to Power Analysis

A Scalable and Programmable Modular Queue Manager Architecture

Regular-Choice Petri Nets for MIMO Detectors

Differential Power Analysis of CAST-128

High-Level Design of a Flexible High-speed FPGA-based Flow Monitor for Next Generation Networks
Acceleration Of HMM-Based Speech Recognition System By Parallel FPGA Gaussian Calculation

Adapting noisy speech models – extended uncertainty decoding

A programmable architecture for layered multimedia streams in IPv6 networks

Replacing Uncertainty Decoding with Subband Re-Estimation for Large Vocabulary

SoC memory hierarchy derivation from dataflow graphs

An Attack-Resilient Sampling Mechanism for Integrated IP Flow Monitors

A Traffic Manager for Integrated Queuing and Scheduling of Unicast and Multicast IP Traffic

Reconfigurable Computing: Architectures, Tools and Applications

FPGA-Based Implementation of Signal Processing Systems

Rapid Design of a Single Chip Adaptive Beamformer

Robustness in digital hardware

Towards a real-time implementation of a physical modeling based percussion synthesizer

From bit level systolic arrays to HDTV processor chips

Power Efficient Dynamic-Range Utilisation for DSP On FPGA

Lecture Notes in Computer Science: Preface

Combining noise compensation and missing-feature decoding for large vocabulary speech recognition in noise
Power Efficient DSP Datapath Configuration Methodology for FPGA

Memory-Centric Hardware Synthesis from Dataflow Models

Towards a real-time implementation of a physical modelling based percussion synthesizer

A Distributed Network Monitor for Flow Detection and Classification

A real-time flow monitor architecture encompassing on-demand monitoring functions

Algorithmic Factorisation for Low Power FPGA Implementations Through Increased Data Locality

QR Recursive Least Squares IP Core Example

Reconfigurable Computing: Architectures, Tools and Applications

Novel percussive instrument design - Converting mathematical formulae into engaging musical instruments

Physical models and musical controllers: Designing a novel electronic percussion instrument

Soft IP core implementation of recursive least squares filter using only multiplicative and additive operators

Design Methodology for Real-Time FPGA-Based Sound Synthesis

Editorial: Transforming signal processing applications into parallel implementations

Programmable network functionality for improved QoS of interactive video traffic

Programmable SoC processor for video object recognition and tracking applications

SoC Memory Hierarchy Derivation from Dataflow Graphs
Rapid Implementation and Optimisation of DSP Systems on FPGA-Centric Heterogeneous Platforms
13 p.

DESIGN METHODOLOGY FOR A BLOCK MOTION ESTIMATION IP CORE

Muir Hardware Synthesis for Multimedia Applications

Multidimensional DSP Core Synthesis for FPGA

Providing Input-Output Throughput Guarantees in a Buffered Crossbar Switch

Hierarchical Synthesis of Complex DSP Functions Using IRIS

Improving the delivery of Interactive Video over QoS enabled IP Networks

From bit level systolic arrays to HDTV processor chips

Parallel implementation of finite difference schemes for the plate equation on a FPGA-based multi-processor array

FPGA Core Network Implementation and Optimization: A Case Study

FPGA-based hardware for physical modelling sound synthesis by finite difference schemes

FPGA-based physical modeling hardware for musical sound synthesis

Programmable Network Functionality for Improved QoS of Interactive Video Traffic

Dataflow-based design methodology for DSP SoC systems

Rapid Implementation and Optimisation of DSP Systems on SoPC Heterogeneous Platforms
Implementation of finite difference schemes for the wave equation on FPGA

Novel Network Functionality for Interactive layered MPEG-4 Video Conferencing

Rapid Generation of Hardware Functionality in Heterogeneous Platforms

High Speed FPGA-based implementations of Delayed-LMS filters

Virtex FPGA Implementation of a Pipelined Adaptive LMS Predictor for Electronic Support Measures Receivers

A Novel Packet Marking Function for Real-Time Interactive MPEG-4 Video Applications in a Differentiated Services Network

Guest Editorial: Cryptography algorithms and architectures for System-on-Chip

LMS Coefficient Filtering for Time-Varying Chirped Signals

Highly efficient, limited range multipliers for LUT-based FPGA architectures

Synthesis and High Level Optimisation of Multidimensional Dataflow Actor Network on FPGA

Embedded Context Aware Hardware Component Generation for Dataflow System Exploration

Guest Editorial: Field Programmable Logic

Clear future direction

Hierarchical synthesis of complex DSP functions on FPGAs

A Parameterisable Motion Estimation Core
Design of a Parameterizable Silicon Intellectual Property Core for QR-Based RLS Filtering

Design Technologies for DSP Algorithm Implementation on Heterogeneous Architectures

Hierarchical DSP architectural synthesis and scheduling solution for "IRIS"

Design flow for efficient FPGA reconfiguration

FPGA-based System-level design framework based on the IRIS synthesis tool and System Generator

High sampling rate retimed DLMS filter implementations in Virtex-II FPGA

Mapping multi-mode circuits to LUT-based FPGA using embedded MUXes

Multiplier-less realization of a poly-phase filter using LUT-based FPGAs

Tracking performance of leakage LMS for chirped signals

Programmable Logic and Applications

Virtex implementation of pipelined adaptive LMS predictor in electronic support measures receiver

Advances in Adaptive Signal Processing: Totally Adaptive Systems

Development of a Run-Time Reconfiguration System with Low Reconfiguration Overhead

Implementation of fixed DSP functions using the reduced coefficient multiplier

Low-power synthesis flow for regular processor design
Low-power synthesis flow for regular processor design

Virtex FPGA implementation of a polyphase filter for sample rate conversion

Advances in adaptive signal processing: Totally adaptive systems

High-performance fine-grained pipelined LMS algorithm in virtex FPGA

An investigation of reconfigurable multipliers for use in adaptive signal processing

Low Power Implementation of a Discrete Cosine Transform IP core

Rapid Design of a Single Chip Adaptive Beamformer

Multiplier based reconfiguration for virtex multipliers

Linear QR architecture for a single chip adaptive beamformer

A virtual hardware handler for RTR systems

Accelerating run-time reconfiguration on FCCMs

A virtual hardware handler for run-time reconfiguration systems

Novel mapping of a linear QR architecture

Image processing chip for small object detection

Low power design of signal processing systems using characterization of silicon IP cores
Parameterizable QR core

Buffer architectures for predictable Quality of Service at the ATM layer

Image compression algorithms using re-configurable logic

Rapid design of a single chip adaptive beamformer

Chip design for high-performance DSP

The impact of data characteristics and hardware topology on hardware selection for low power DSP

Accelerating run-time reconfiguration on custom computing machines

A programmable image processing chip

Fast partial reconfiguration for FCCMs

Analysis of ATM switch design for achieving predictable quality of service

Impact of data characteristics and hardware topology on hardware selection for low power DSP

Preserving quality of service in wireless ATM networks

Programmable image processing chip

Rapid design of a single chip adaptive beamformer

Applying an XC6200 to real-time image processing
Implementation of the 2D DCT using a XILINX XC6264 FPGA

Architectural synthesis of digital signal processing algorithms using "IRIS"

FPGA synthesis on the XC6200 using IRIS and Trianus/Hades (or from heaven to hell and back again)

Error analysis of FFT architectures for digital video applications

VLSI architectures for field programmable gate arrays: A case study

64-point Fourier transform chip for digital television applications

Architectural strategies for implementing an image processing algorithm on XC6000 FPGA

Architectural synthesis and efficient circuit implementation for field programmable gate arrays

Error analysis of FFT architectures for digital video applications

New FFT architecture and chip design for motion compensation based on phase correlation

Optimised multiply/accumulate architecture for very high throughput rate digital filters

Programmable high-performance IIR filter chip

Real-Time Emulation of Fault Management functions within an SDH Network

Architectural synthesis of an image processing algorithm using IRIS
High performance IIR filter chip and its evaluation system

Real-Time modelling of Alarm Generation and Propagation in an SDH Network

Novel VLSI implementation of (8×8) point 2-DDCT

High performance DSP ASIC for multiply, divide and square root

The design of a VLSI array processor chip for computing the basic arithmetic operations

Saturation circuitry for redundant number based hr filters

High performance VLSI architecture for division and square root

VLSI Systems for DSP and Control

Optimized bit level architectures for IIR filtering

Bit-Level systolic architectures for high performance IIR filtering

Pipelined two-port adaptor for wave digital filtering

Systolic array architectures for parameterised multiplexed IIR filters

A high performance IIR digital filter chip

Bit-level systolic architecture for very high performance IIR filters
A high performance systolic IIR filter architecture

Bit-level systolic arrays for IIR filtering.

Systolic building block for high performance recursive filtering

SYSTOLIC IIR FILTERS WITH BIT LEVEL PIPELINING.

Projects
R1898ECI: Adaptive Hardware Systems with Novel Algorithmic Design and Guaranteed Resource Bounds
Woods, R.
01/08/2007 → …

R1701ECI: CASE award: M.S. McKeown- EPSRC/SELEX
Woods, R.
01/08/2005 → …

R1848ELE: Dorothy Hodgkin Postgraduate Award
Woods, R.
01/08/2006 → …

R1318ECI: eFUTURES XD
Woods, R.
01/08/2011 → 27/05/2015

R1057ECI: eFutures2 : exploiting the UK's rich heritage in electronics
Woods, R.
15/04/2019 → …

R1337CSC: ENPOWER
Nikolopoulos, D. & Woods, R.
01/08/2013 → 05/02/2018

R1603ELE: EPSRC Case Ref 0430024 - Hasson
Woods, R.
01/08/2004 → …

R1917CNR: Health Data Research UK (HDR UK)
Lawler, M., Blayney, J., Coleman, H., Dunne, P., Heaney, L., Kee, F., McArt, D., Nikolopoulos, D., O'Reilly, D., Overton, I., Salto-Tellez, M. & Woods, R.
29/10/2018 → …

R1129ECI: Kelvin-2 - The High Performance Computing Centre in Northern Ireland (HPC-NI)
R6410CSC: NanoStreams: A Hardware and Software Stack for Real-Time Analytics on Fast Data Streams
Nikolopoulos, D., Spence, I. & Woods, R.
01/08/2013 → …

R6551CSC: Open TransPRecision COMPuting
Woods, R., Karakonstantis, G. & Vandierendonck, H.
03/11/2016 → …

R1138ECI: Programmable embedded platforms for remote and compute intensive image processing applications
Woods, R.
01/08/2012 → 31/07/2017

R1722CMM: Queen's University Belfast Imaging and Patterning Centre
Gregg, M., McNeill, D., Mitchell, N. & Woods, R.
20/02/2017 → 31/03/2018

R1728ELE: SHARES- System-on-chip heterogeneous architecture recognition engine for speech
Woods, R. & Ji, M.
01/08/2005 → …

R1128CSC: Softcore Streaming Processors for FPGA DSP
McAllister, J. & Woods, R.
01/08/2009 → 28/02/2014

Woods, R.
01/08/2007 → …

R1307ECI: WifiEar: A New Form of Telecoil
Woods, R. & Marshall, A.
01/08/2012 → …

Awards

Activities

Meeting The Challenges of an Ageing Society
Roger Woods (Advisor)
17 Feb 2020

Big Data conference
Roger Woods (Participant)
24 Oct 2019

15th International Symposium on Applied Reconfigurable Computing
Roger Woods (Conference committee co-chair)
01 May 2019

Big Data Week
Roger Woods (Chair)
18 Oct 2018
26th European Signal Processing Conference
Roger Woods (Member of programme committee)
03 Sep 2018 → 07 Sep 2018

International Conference on Field Programmable Logic and Applications
Roger Woods (Member of the organising committee)
27 Aug 2018 → 31 Aug 2018

UK Research and Innovation (External organisation)
Roger Woods (Advisor)
20 Aug 2018 → …

IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation
Roger Woods (Member of programme committee)
15 Jul 2018 → 19 Jul 2018

14th International Symposium on Applied Reconfigurable Computing (Event)
Roger Woods (Board Member)
02 May 2018

Big Data conference
Roger Woods (Chair)
19 Oct 2017

Big Data Week
Roger Woods (Chair)
17 Oct 2017

IEEE International Workshop on Signal Processing Systems
Roger Woods (Member of programme committee)
03 Oct 2017 → 05 Oct 2017

FPL2017
Roger Woods (Member of programme committee)
04 Sep 2017 → 08 Sep 2017

17th International Conference on Embedded Computer Systems: Architectures, Modelling and Simulation
Roger Woods (Participant)
17 Jul 2017 → 20 Jul 2017

eFutures Annual Community Event
Roger Woods (Participant)
23 May 2017

International Symposium on Applied Reconfigurable Computing
Roger Woods (Member of programme committee)
03 Apr 2017 → 07 Apr 2017

IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Journal)
Roger Woods (Peer reviewer)
14 Mar 2017
FPL2017
Roger Woods (Advisory board member)
2017

Key Generation from Wireless Channels
Roger Woods (Invited speaker), Alan Marshall (Invited speaker), & Junqing Zhang (Invited speaker)
08 Dec 2016

Key Generation from Wireless Channels
Roger Woods (Invited speaker)
04 Dec 2016 → 08 Dec 2016

IEEE International Workshop on Signal Processing Systems
Roger Woods (Member of programme committee)

International Conference on Field-Programmable Logic and Applications
Roger Woods (Member of programme committee)
29 Aug 2016 → 02 Sep 2016

16th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation
Roger Woods (Member of programme committee)
17 Jul 2016 → 21 Jul 2016

Roger Woods (Member of programme committee)
17 Jul 2016 → 21 Jul 2016

Big Data Week
Roger Woods (Chair)
02 Jun 2016

Big Data conference
Roger Woods (Chair)
20 May 2016

International Conference on Field-Programmable Logic and Applications
Roger Woods (Advisory board member)
2016

IEEE International Workshop on Signal Processing Systems
Roger Woods (Member of programme committee)
14 Oct 2015 → 16 Oct 2015

International Conference on Field-Programmable Logic and Applications
Roger Woods (Member of programme committee)
02 Sep 2015 → 04 Sep 2015

IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation
Roger Woods (Member of programme committee)
20 Jul 2015 → 23 Jul 2015

FPGA-based acceleration of data applications
Roger Woods (Advisor)
11 May 2015
Big Data Conference
Roger Woods (Chair)
23 Apr 2015

48th Asilomar Conference on Signals, Systems and Computers
Roger Woods (Chair)
02 Nov 2014 → 05 Nov 2014

IEEE Workshop on Signal Processing Systems
Roger Woods (Member of the organising committee)

Entrepreneurship in practice in a university setting
Roger Woods (Advisor)
16 Oct 2014

Roger Woods (Advisor)
06 Oct 2014

Workshop on FPGA-based Implementation of Signal Processing Systems
Roger Woods (Participant)
23 Jun 2014 → 27 Jun 2014

Big Data Week
Roger Woods (Chair)
07 May 2014

Research Excellence Framework (REF) (External organisation)
Roger Woods (Member)
2014

IEEE International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation
Roger Woods (Vice chair)
15 Jul 2013 → 18 Jul 2013

Engineering & Physical Sciences Research Council (External organisation)
Roger Woods (Chair)
29 May 2013

Engineering & Physical Sciences Research Council (External organisation)
Roger Woods (Member)
06 Feb 2013

Novel architectures and design tools for the implementation of complex DSP systems on FPGA-based technologies
Roger Woods (Speaker)
08 Nov 2012

IEEE Signal Processing Summer School
Roger Woods (Organiser)
20 Aug 2012 → 24 Aug 2014
Research Excellence Framework (REF) Panel (External organisation)
Roger Woods (Member)
01 Apr 2011 → 31 Dec 2014

International Workshop on Applied Reconfigurable Computing
Roger Woods (Chair)
23 Mar 2011 → 25 Mar 2011

Engineering Policy Group Northern Ireland (External organisation)
Roger Woods (Vice Chair)
2011 → …

EPSRC Associate Peer Review College (External organisation)
Roger Woods (Member)
2011 → …

eFutures (External organisation)
Roger Woods (Board Member)
2010 → …

Microelectronics Design Grand Challenges: uGC1: Batteries Not Included
Roger Woods (Member)
23 Nov 2009

International Conference on Wireless Communications and Signal Processing, Nanjing, China
Roger Woods (Keynote/plenary speaker)
13 Nov 2009

17th European Signal Processing Conference (EUSIPCO-2009)
Roger Woods (Invited speaker)
27 Aug 2009

International Workshop on Applied Reconfigurable Computing
Roger Woods (Chair)
16 Mar 2009 → 18 Mar 2009

Analytics Engines Limited (External organisation)
Roger Woods (Board Member)
2007 → …

Roger Woods (Board Member)
2007 → …

ACM Transactions on Reconfigurable Technology and Systems (Journal)
Roger Woods (Editorial board member)
2006

ACM Transactions on Reconfigurable Technology and Systems (Journal)
Roger Woods (Associate editor)
2005 → …

EURASIP Journal on Signal Processing (Journal)
Roger Woods (Editorial board member)
2004 → 2007

**Journal of VLSI signal processing systems for signal, image and video technology (Journal)**
Roger Woods (Editorial board member)
2003 → …

**IET COMPUTERS AND DIGITAL TECHNIQUES (Journal)**
Roger Woods (Associate editor)
2001 → …

**Press clippings**

A conversation with Analytics Engines' and Queen's University's Roger Woods
Roger Woods
01/09/2017
1 Media contribution

Analytics Engines | Stephen McKeown | Invest NI Support
Roger Woods
08/05/2013
1 Media contribution

Big Data conference is a Titanic success
Roger Woods
20/10/2017
1 Media contribution